

Fault-tolerant circuit synthesis for universal fault-tolerant quantum computing

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We present a quantum circuit synthesis algorithm for implementing universal fault-tolerant quantum computing based on concatenated codes. To realize fault-tolerant quantum computing, the fault-tolerant quantum protocols should be transformed into executable quantum circuits based on the nearest-neighbor interaction. Unlike topological codes that are defined based on local operations fundamentally, for the concatenated codes, it is possible to obtain the circuits composed of the local operations by applying the quantum circuit synthesis. However, by the existing quantum circuit synthesis developed for ordinary quantum computational algorithms, the fault-tolerant of the protocol may not be preserved in the resulting circuit. Besides, we have to consider something more to implement the quantum circuit of universal fault-tolerant quantum computing. First, we have not to propagate quantum errors on data qubits when selecting a qubit move path (a sequence of *SWAP* gates) to satisfy the geometric locality constraint. Second, the circuit should be self-contained so that it is possible to act independently regardless of the situation. Third, for universal fault-tolerant quantum computing, we require multiple fault-tolerant quantum circuits of multiple fault-tolerant quantum protocols acting on the same input, a logical data qubit. Last, we need to recall fault-tolerant protocols such as syndrome measure and encoder implicitly include classical control processing conditioned on the measurement outcomes, and therefore have to partition the quantum circuits in time flow to execute the classical control as the architect

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intended. We propose the circuit synthesis method resolving the requirements and show how to synthesize the set of universal fault-tolerant protocols for $[[7, 1, 3]]$ Steane code and the syndrome measurement protocol of $[[23, 1, 7]]$ Golay code.

1 Introduction

An $[[n, k, d]]$ quantum error-correcting code encodes a k -qubit logical quantum information into n physical (or lower concatenation level) qubits, and protects the encoded information from at most $\lfloor (d-1)/2 \rfloor$ -qubit arbitrary quantum error, where d is the code distance of the code. If the number of arbitrary quantum errors is not more than $\lfloor (d-1)/2 \rfloor$, it is possible to detect and correct the quantum errors. Otherwise, the logical information encoded into the code is broken, and cannot be recovered.

A quantum computing protocol acting on an error-corrected logical qubit is called *fault tolerant* if the probability that the logical qubit is corrupted by quantum noise during running the protocol is suppressed than that in the non-error-corrected quantum computing. For that, there should be no chance that arbitrary quantum errors to propagate to more than $\lfloor (d-1)/2 \rfloor$ qubits within the logical qubit in the protocol. By the way, we need to say that some physical qubits composing the logical qubit are more important than others. The qubits those must not be affected by quantum error to keep the fault tolerance are the qubits, called as *data qubit*, holding quantum data. Therefore, a fault-tolerant quantum computing is not broken even if some qubits that do not belong to data qubits are corrupted by quantum errors. By having a noisy interaction with data qubits, the quantum errors on the ancilla qubits are propagated to the data qubits, and the encoded qubit will become corrupted if the

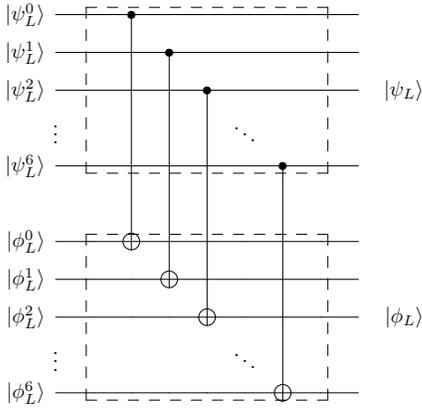


Figure 1: Transversal gate implementation of a logical CNOT gate

number of the data qubits where error happened is greater than $\lfloor (d-1)/2 \rfloor$. Therefore, to retain the fault tolerance, we have to block the error propagation over the data qubits within the encoded logical qubit.

Needless to say, a fault-tolerant quantum computing protocol is designed by keeping in mind the rule that does not allow interactions that are likely to be noisy between the data qubits. A transversal implementation of a logical gate is a typical approach for the fault tolerance (see Figure 1). However, the fact that a protocol has fault tolerance itself does not guarantee that the protocol can be executed in a fault-tolerant way in practice. A fault-tolerant protocol should be transformed into a fault-tolerant quantum circuit that is executable in the practical situation governed by the geometric locality constraint. In the transformation, to resolve the constraint that a quantum computing device has, all the multi-qubit quantum gates in the protocol have to be decomposed into a sequence of the local 2-qubit gates acting on the nearest neighbor qubits. The decomposition can be achieved by introducing a sequence of quantum state move (*SWAP* gates) between distant qubits.

The transformation from the protocol (algorithm) to an executable circuit is called a *circuit synthesis* or *circuit mapping*, and so far a lot of quantum circuit mapping algorithms have been proposed. Most quantum circuit synthesis algorithms makes an executable quantum circuit by including as least qubit move as possible by exploiting the qubit connectivity of the quantum device, but some advanced methods [1, 2] additionally consider the real performance of the target quantum device

such as the fidelity or the execution time of physical gates.

Back to the fault-tolerant quantum protocol, to implement the circuit of the protocol, we have to consider more than the requirements in the circuit synthesis for an ordinary quantum algorithm. As mentioned above, a normal circuit synthesis is designed to resolve the locality constraint by introducing the qubit move via *SWAP* gates as little as possible. For that, the type of quantum information a physical qubit holds is out of concern. If such a circuit synthesis method is applied to a fault-tolerant quantum protocol, obviously it generates a quantum circuit including as few *SWAP* gates as possible. By the way, the serious problem here is that the circuit may include *SWAP* gates acting on both data qubits. As mentioned before, a noisy *SWAP* gate may make both the data qubits corrupted. Therefore, in the circuit synthesis on a fault-tolerant quantum protocol, a *SWAP* gate between the data qubits should be selected very limitedly.

In addition, there are additional issues to take into account for the circuit synthesis for universal fault-tolerant quantum computing. We need the fault-tolerant circuits for multiple fault-tolerant quantum protocols, and each circuit has to work correctly regardless of the situation. Besides, some fault-tolerant quantum protocols such as syndrome measurement involve classical operations conditioned on the result of quantum operations. Therefore, to implement their circuits exactly as designed, we have to clearly specify the turn for the digital operations in their circuits.

As far as the authors know, nothing has been proposed for the circuit synthesis algorithm specialized for universal fault-tolerant quantum computing, in particular, based on the concatenated codes. Only for a few well-known codes, some results obtained manually for studying thresholds have been reported [3–5]. Those results may be optimal for the designated target environment, but for another setting or quantum code, it is not easy to find fault-tolerant circuits by applying their methodology. For this reason, we believe a circuit synthesis method specialized in fault-tolerant quantum protocols is required.

In the present work, we propose a fault-tolerant circuit synthesis algorithm for universal fault-tolerant quantum computing. As mentioned above,

the algorithm selectively picks *SWAP* gates according to the type of quantum information physical qubits store when selecting the qubit move path. We call the qubit move not including (or including very limitedly) the *SWAP* gates acting on the data qubits as *fault-tolerant qubit move*. By taking the fault-tolerant qubit move path, it is possible to retain the fault-tolerance originating from the protocol in the resulting circuit. However, the fault-tolerant qubit move path itself is not enough for realizing universal fault-tolerant quantum computing.

As is well known, to realize universal fault-tolerant quantum computing, we need multiple fault-tolerant logical gates (H , T , and $CNOT$), syndrome measurement, and encoding protocol. According to a quantum code, a fault-tolerant protocol to prepare or distill a special logical ancilla state is also necessary. That is, we have to obtain the fault-tolerant circuits of all the above-mentioned protocols. The most important things for the circuit mapping over the multiple fault-tolerant protocols are first most protocols act on the same configuration of a logical qubit, and second, during the fault-tolerant quantum computing the protocols are applied repeatedly. Note that the configuration of a logical qubit indicates the arrangement of physical data qubits in a logical qubit (please see Figure 16). For the above considerations, the proposed algorithm shares the configuration of a logical qubit for the circuit synthesis over all the protocols and makes the resulting circuit *self-contained* so that it can act independently regardless of the situation. The details will be discussed in the main body.

Lastly, as mentioned above, to run a fault-tolerant quantum protocol as designed, we have to include the execution of classical processing implicitly contained in the protocol. For that, we need implement a single fault-tolerant quantum protocol as multiple small fault-tolerant circuits and run the classical operation between the circuits. In the present work, we achieve it in two directions. First, one inserts *barrier* statements in the protocol and the circuit synthesis deals with them. The position where the statements are inserted is, on considering an ordinary fault-tolerant protocol structure, when all the ancilla qubits that were prepared within the protocol are measured. Second, we first partition the protocol into several sub-protocols and conduct the circuit synthesis on each sub-protocol individu-

ally, but with sharing information common to them.

The proposed circuit synthesis algorithm is based on the heuristic circuit mapping algorithm, SABRE (SWAP-based Bi-directional heuristic search algorithm) [6]. The most important reasons we hire the algorithm for our purpose are first it is possible to easily take the type of quantum information each qubit holds into account to find the qubit move path, and second, as discussed in the literature, it works more efficiently than other global optimization methods.

The remainder of this paper first briefly describes SABRE. We then discuss the four requirements of the circuits for universal fault-tolerant quantum computing, propose our ideas for them, and describe how to implement the ideas with SABRE. As an example, we show the full snapshots of the syndrome measurement circuit of $[[7, 1, 3]]$ Steane code in sequence. We then go into the full set of universal fault-tolerant quantum circuits based on Steane code obtained by applying our algorithm. As the last example, we show the circuit of the syndrome measurement of $[[23, 1, 7]]$ Golay code that is well known as having a high error correction threshold among the concatenated codes.

2 Review of SABRE

We review the heuristic quantum circuit mapping algorithm SABRE in the present section. The algorithm generates a quantum circuit believed to be optimal by iterating the procedure composed of picking a random qubit initial mapping and finding the gate sequence based on that mapping as many times as possible. The standard of the optimality can be flexibly adopted, the number of quantum gates, the circuit depth, or anything.

The main procedure of SABRE which is to find the gate sequence is composed of iterating graph traversals three times in the alternating directions (forward, backward and forward again), where the graph is formed as a directed acyclic graph (*DAG*) from a quantum algorithm. For the graph traversals in the forward and backward directions, the graph also should be made for both directions respectively. Note that a node in DAG includes a quantum instruction of a quantum gate and qubits where the gate acts. Figure 2 shows the running flow of SABRE.

In the graph traversal for the forward (backward)

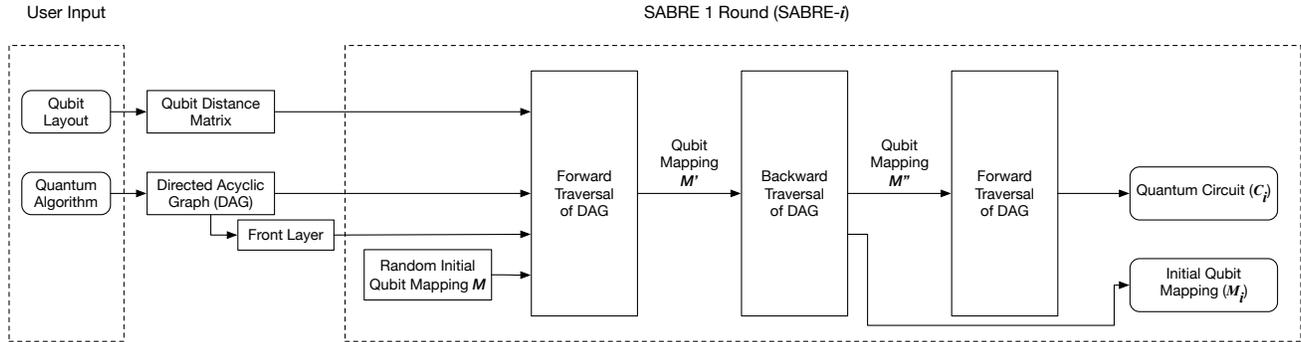


Figure 2: The architecture of SABRE [6]. The user inputs, *Qubit Layout* and *Quantum Algorithm*, are common to all the iterations. Usually, *Qubit Layout* is provided as a physical qubit coupling graph of a quantum chip and *Quantum Algorithm* is given in the QASM format ([7]). Provided *Qubit Layout* and *Quantum Algorithm*, how to make *Qubit Distance Matrix* and *Directed Acyclic Graph* are well described in the literature. The algorithm is composed of multiple iteration of SABRE graph traversals. Each iteration begins by picking an initial qubit layout randomly. After conducting the i -th iteration of SABRE (SABRE- i), we will have a quantum circuit (C_i) and the associated initial qubit mapping table (M_i). The optimal quantum circuit and its associated initial qubit mapping will be obtained by comparing all the results.

direction, the algorithm checks whether each node of the DAG that is generated for the corresponding traversal is executable with respect to the qubit layout of a given quantum chip, and finds required a local optimal *SWAP* quantum gate to make un-executable node executable. Please note that a quantum gate is called *executable* if it acts locally on the given qubit layout (quantum chip). An optimal *SWAP* gate is selected from the evaluation of the cost of all the *SWAP* candidate gates which are chosen based on the qubits where the above-mentioned un-executable nodes (gates) act.

The graph traversal is composed of the following two steps.

1. Find any executable gates in *Front Layer*
2. Append all the executable gates to the circuit or Find a *SWAP* gate if there does not exist any executable gates

Note that *Front Layer* (FL) is defined as the set of root nodes in the DAG.

If a node in FL, $node_a$, is executable, then it is removed from FL (and DAG) and is appended to the resulting quantum circuit. In general, the node has succeeding nodes in DAG, and suppose that a node $node_b$ is such one. Note that $node_b$ belongs to DAG but not in FL. $node_b$ then has preceding nodes, some of them are already exported to the circuit and the others are not. If, after exporting $node_a$ to the circuit, none of the preceding nodes of $node_b$ remain in FL, we pull $node_b$ from non-FL to FL.

Otherwise, if none in FL is executable, the algorithm collects several candidate *SWAP* gates and selects an optimal one from the cost evaluation. Then, by moving qubits via the selected *SWAP* gates, some gates in FL may become executable or close to executable one. The qubit mapping status is also updated by the *SWAP* operation. In the literature, two kinds of the cost function are defined, but the heart of both is the same as they evaluate the total qubit move distance to make all the nodes in FL executable. The graph traversal is terminated if FL becomes empty, that is, when all the nodes of DAG are appended to the quantum circuit.

After each graph traversal is done, the changed qubit mapping table is passed to the next graph traversal in general (see Figure 2). Therefore, the initial qubit mapping and the resulting quantum circuit of the last graph traversal become the qubit mapping and the quantum circuit of a current SABRE round. The performance of a quantum circuit obtained in each round is affected by the initial qubit mapping chosen randomly. Therefore, the more iterations, the better performance of a quantum circuit.

3 Circuit Synthesis for Universal Fault-Tolerant Quantum Computing

This section raises four requirements for implementing the quantum circuits for universal fault-tolerant quantum computing. The first is about how to

block the error propagation over the data qubits, the second is about how to make self-contained quantum circuits so that they can be executed independently regardless of situations, and the third is about how to prepare a whole set of fault-tolerant quantum circuits for universal quantum computing. The last one is about how to execute the fault-tolerant quantum circuits including classical processings in practice.

3.1 Fault-tolerant qubit move

Previously, we have mentioned that a protocol has the fault-tolerance if the number of quantum errors happened on data qubits is bounded by the capacity of quantum error correction. In this section, we first propose an idea to block the error propagation over the data qubits and then discuss how to implement the method into SABRE. A logical qubit encoded by an $[[n, k, d]]$ quantum error-correcting code contains n data qubits. Besides, in practice, several ancilla qubits for storing error syndrome and verifying the specially prepared ancilla state are additionally needed. Please see the syndrome measurement protocol in Figure 3. There are 7 data qubits $|\psi\rangle_L^i$ and 7 syndrome qubits $|\text{syndrome}^i\rangle$. Even though it is not explicitly described there, additional qubits are required to verify the prepared logical states $|+\rangle_L$ and $|0\rangle_L$ (see Ref. [8]). Therefore, by assuming the reuse of the ancilla qubits, to run the protocol we need at least 15 qubits.

Suppose that the qubits $|\psi\rangle_L^0$ and $|\text{syndrome}^0\rangle$ are geometrically adjacent. Then, the first *CNOT* gate in Figure 3 is executable. Otherwise, to resolve the locality constraint imposed on the quantum device, we need to move qubits to make them placed in the neighbor. What here we need to be careful of is that all the quantum gates exploited in quantum computing are noisy! If a quantum error happens during running a noisy *SWAP* gate acting on two data qubits, both the qubits will be corrupted as

$$\begin{aligned} \widetilde{U_{SWAP}}|\psi\rangle|\phi\rangle &= (I + \epsilon_2) \cdot U_{SWAP}|\psi\rangle|\phi\rangle \\ &= |\tilde{\phi}\rangle|\tilde{\psi}\rangle, \end{aligned}$$

where ϵ_2 is an arbitrary 2-qubit error and U_{SWAP} is an ideal noiseless *SWAP* gate. Therefore, in the circuit synthesis for a fault-tolerant quantum protocol, we have to avoid or limit introducing *SWAP* gates between data qubits for moving the qubits. Note that for computing algorithms, this is out of concern.

We now discuss how to choose *SWAP* gates to implement an executable circuit and not to spread quantum errors over data qubits at the same time. The physical qubits constituting a logical qubit have their own lifetime within fault-tolerant quantum computing. For example, the data qubits hold the quantum data for quantum computing, and therefore their lifetimes are equal to that of the logical qubit. On the other hand, the syndrome qubits only work in the non-trivial way for the duration of the ancilla preparation and the syndrome measurement. Therefore, their lifetimes are the duration of those operations. Then, for the rest, the quantum state they hold is not critical to quantum computing, and therefore they can be played as the communication channel.

We trace the usage status of each qubit within the fault-tolerant quantum protocol. If a qubit is prepared as a certain quantum state $|0\rangle$ (or $|+\rangle$), the usage status of the qubit turns into *activated*. On the other hand, its status becomes *inactivated* if a qubit is measured. During running a fault-tolerant protocol, the usage status of a qubit is changed along the working flow of the protocol. When activated status, a qubit holds significant quantum state for the protocol, but when inactivated it just stores a kind of garbage information. Please see Figure 3.

Regarding the usage status, we classify qubits into data-type qubits and non-data-type qubits. A *data-type* qubit is defined as a qubit in the activated status, and a *non-data-type* qubit is one in the inactivated. As mentioned above, a data-type qubit carries a non-trivial quantum information, but a non-data-type qubit holds a kind of garbage information. Therefore, we have to block or limit *SWAP* gate between the data-type qubits in the circuit synthesis.

As mentioned above, it is not that the *SWAP* gates between the data-type qubits are never allowed. In general, according to the code distance d , it is possible to allow the *SWAP* gates as much as $\lfloor (d-1)/4 \rfloor$ times because arbitrary $\lfloor (d-1)/2 \rfloor$ errors can be recovered. For example, since a quantum code of $d = 5$ can correct arbitrary 2-qubit errors, one-time noisy *SWAP* gate between data qubits does not break a logical qubit.

So far, we have discussed the requirement of how to find the fault-tolerant qubit move by limiting the *SWAP* gates between the data-type qubits.

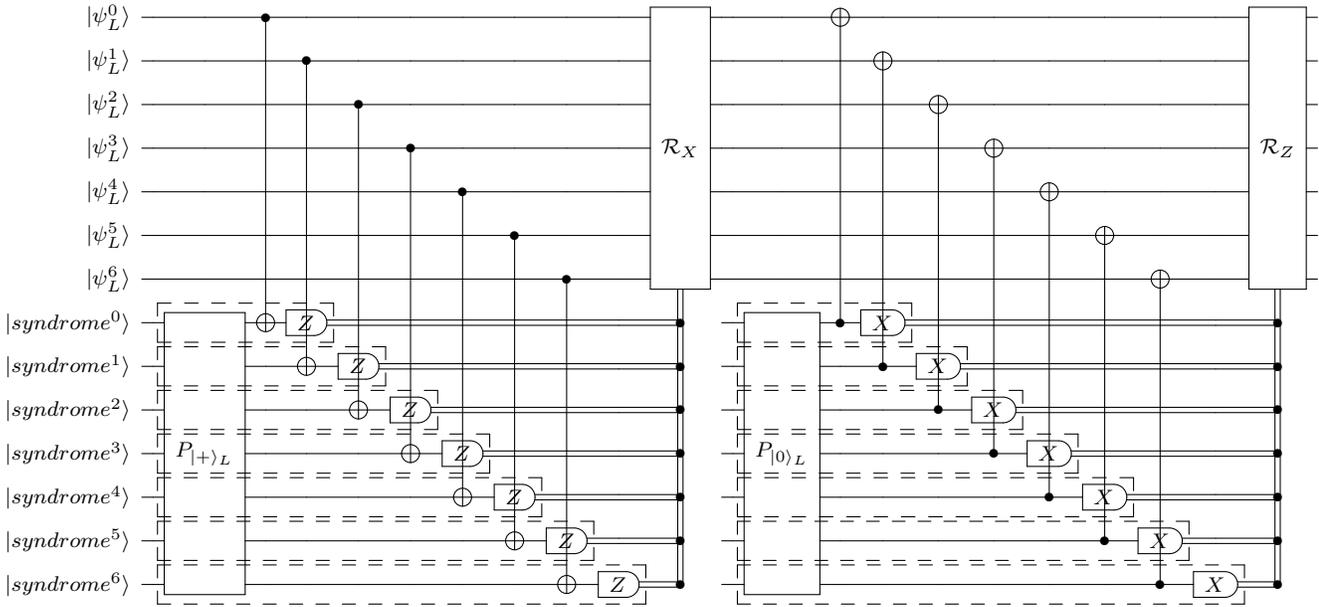


Figure 3: Protocol for the syndrome measurement based on steane QEC method [9]. The dotted boxes for the ancilla qubit $|anc^i\rangle$ are its activation periods. The outsides of the boxes are the inactivation periods. In the forward direction graph traversal, the usage status of each qubit becomes activated by preparation and inactivated by measurement. On the other hand, in the backward direction, the measurement (preparation) operation makes the status of each qubit activated (inactivated). In ideal situation, all the ancilla qubits have the same activation period, but in practice due to the locality, some ancilla qubits have longer activation period than others. Please note that the data qubits $|\psi_L^i\rangle$ are all activated.

Then, it is time to discuss how to implement the method into SABRE. First of all, we need to recall of SABRE is composed of three graph traversals in alternating directions. Previously, we mentioned that the usage status of a qubit becomes activated (inactivated) if it is prepared (measured). Such a rule is based on the normal execution flow of a quantum circuit, that is the forward traversal of DAG. If a quantum circuit is executed in the reverse direction then the status change is triggered by the opposite operation. That is, in the backward traversal of DAG, the status is turned into activated (inactivated) by measurement (preparation).

We have mentioned that the original SABRE collects all the possible *SWAP* gates that act on the qubits of the nodes in FL, and then picks up the optimal one from them. But, in the proposed algorithm, we selectively collect the *SWAP* candidates to limit the *SWAP* gates on the data-type qubits. For that, we first examine the type of the qubits. There are three kinds of qubit pairs: 1) both non-data-type qubits, 2) one data-type qubit and one non-data-type qubit, and 3) both data-type qubits. The first and second cases, needless to say, can be collected as the *SWAP* candidates, but for the third one, we need to do something described in what fol-

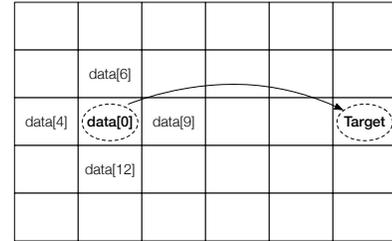


Figure 4: Since the data qubit $data[0]$ is surrounded by data qubits, it can not be moved to another physical qubit in a fault-tolerant way.

lows.

Suppose that for some reason (which will be discussed later in detail) we need to move the quantum state a data-type qubit holds to another qubit. Figure 4 shows that since $data[0]$ is currently surrounded by data-type qubits, the quantum state in $data[0]$ cannot be moved to *Target* without interaction with one data-type qubit. Figure 5 shows another situation where finding a fault-tolerant movement path may fall in an infinite loop. To relieve such traffic jams, we need to move other data-type qubits around $data[0]$ to somewhere beforehand. We then are able to move $data[0]$ to *Target* without interaction with any data-type qubits. In this regard, we collect the *SWAP* gates acting on the

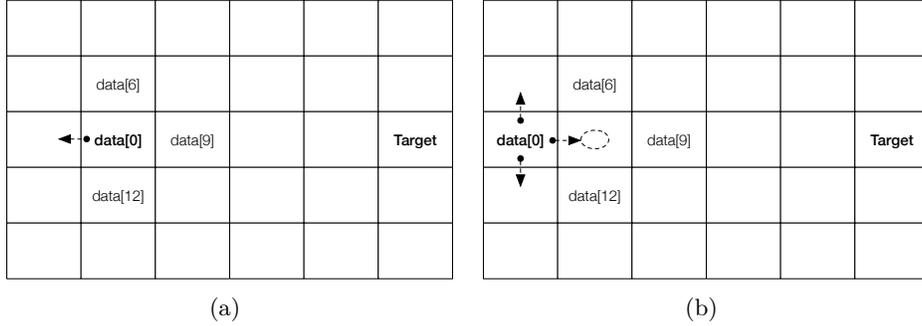


Figure 5: A circuit synthesis falls in an infinite loop when a data qubit surrounded by other data qubits is moved to another place. All the cells indicate physical qubits. (a) $data[0]$ has only one option for the next move, which is the left cell of which. (b) The cost function based on the distance between qubits selects the b cell for the next move.

qubits that are positioned next to the data-type qubit $data[0]$ as *SWAP* candidates. Figure 6 shows the effect of this rule.

Previously, we mentioned that the *SWAP* gate between both the data-type qubits can be allowed as much as $\lfloor (d-1)/4 \rfloor$ times. For that, in the beginning, we designate the number of maximally allowed interactions between data-type qubits as $allowable_max_interaction = \lfloor (d-1)/4 \rfloor$, where d is the code distance. Then, when collecting the *SWAP* candidates we can add a *SWAP* gate acting on a pair of both data-type qubits if the number of the allowed interaction so far is less than the pre-determined limit. Later, after cost evaluation on the *SWAP* candidates, if the *SWAP* gate acting on both the data-type qubits is chosen as an optimal one, we then increment the number of the allowed interaction by 1.

The quantum circuit generated by the rule we have mentioned so far includes very limited interactions between data-type qubits. Therefore, a quantum error that happened randomly does not propagate to data qubits beyond the capacity of the quantum error correction. Then, we can say that the circuit works in the fault-tolerant manner. However, it is not enough for universal fault-tolerant quantum computing. In the following subsections, we raise additional requirements and propose our solutions for them.

3.2 Self-contained quantum circuit

Suppose that you have a fault-tolerant quantum circuit and its initial qubit mapping table of the syndrome measurement protocol by applying the method described in the previous section. Then,

it is possible to measure the error syndrome by running the circuit to a logical qubit if the logical qubit is configured like the initial qubit mapping table. Otherwise, if the logical qubit is not formed as the mapping table, the circuit does not work as intended. Needless to say that the quantum circuit should be consistent with the initial qubit mapping.

Fault-tolerant quantum computing performs error correction periodically. Then, does the fault-tolerant circuit obtained above always work correctly for the fault-tolerant quantum computing? Unfortunately, it does not. The circuit works correctly for one time only, the first time. The reason is as follows. If a quantum circuit includes *SWAP* gates introduced by the circuit synthesis, by executing the circuit the qubit mapping will become different from the initial mapping. Therefore, running the circuit again on the logical qubit will make the output different than expected because the initial mapping for the circuit is not fulfilled. Please see Figure 7. Please note that *SWAP* gates originally included in the protocol itself do not raise such problems.

Therefore, to make the syndrome measurement circuit work always correctly throughout the fault-tolerant quantum computing, after obtaining the syndrome values we have to move the physical qubits in the logical qubit back to their initial positions. In the present work, we call the circuit that always works correctly regardless of the situation a *self-contained* circuit. For that, our algorithm automatically moves the data qubits to the designated positions after the main body of a fault-tolerant protocol. Please note that since the lifetimes of the ancilla qubits are bounded by a protocol, we only focus on the data qubit (not data-type qubit) for

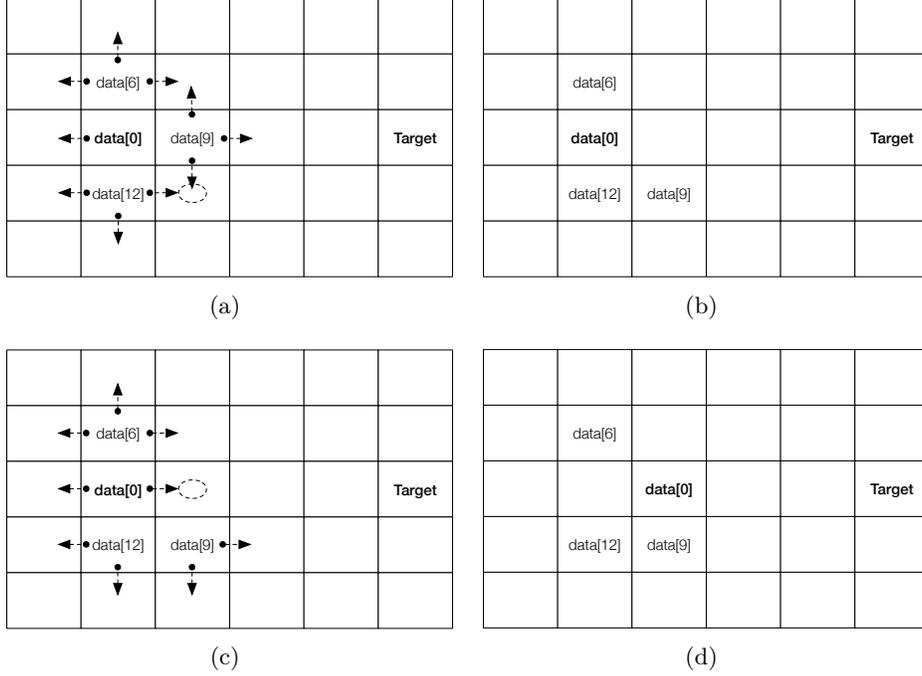


Figure 6: By first moving the data-type qubits located around the qubit that has to move to the destination, the traffic jams shown in Figures 4 and 5 can be relieved and it becomes possible to find a fault-tolerant movement path. (a) Collect *SWAP* gates from both the data-type qubit and its neighbor data-type qubits. (b) Based on the cost evaluation, *data[9]* is moved to its neighbor cell of the dotted circle. (c) Collect *SWAP* gates from both the data-type qubit and its neighbor data-type qubits. (d) Based on the cost evaluation, *data[0]* moves toward the destination *Target* without interaction with any data-type qubits.

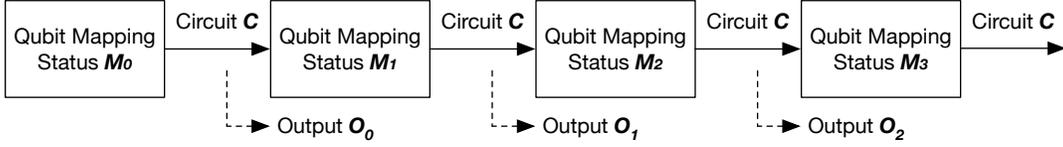


Figure 7: The repetitive execution of a quantum circuit including *SWAP* gates introduced by circuit mapping does not work as expected because of the qubit mapping problem, ($O_0 \neq O_1 \neq O_2 = \dots$).

the self-contained property.

To implement the move operation into SABRE, we automatically add the instruction “*Move data[i] destination[i]*” for all the data qubits before generating DAG (see Figure 2). The first argument *data[i]* is the name of a data qubit used in the protocol, and the second argument *destination[i]* is the destination of the move. *destination[i]* can be a specific physical qubit index or a symbolic value. However, even if it is provided as a symbolic value in the beginning it is translated to a specific index as the circuit mapping proceeds.

We now describe how to deal with the operation *Move* in the proposed algorithm. SABRE basically examines whether a quantum instruction in FL is executable or not based on the geometric locality.

In the case of a *CNOT* (or *SWAP*) gate, it determines as executable if a control qubit is positioned next to a target qubit. On the other hand, for the *Move*, we check whether the argument qubit is located at the designated position or not. If the *Move* is executable, then the algorithm does not do anything after removing it in FL. Note that if a *CNOT* gate is executable, then it is exported to the circuit.

In this work, the operation that moves all the data qubits to the designated position is called *Move-Back* because the target position is usually its initial location. The necessity of the *Move-Back* depends on a fault-tolerant protocol. Here we describe the details of the *Move-Back* for the syndrome measurement protocol, and other protocols will be discussed in the following section.

In the present work, we assume that after the syndrome measurement a logical gate acts on a logical qubit without additional operation. For that, the arrangement of all the component qubits of a logical qubit after the syndrome measurement should be the same as the initial one of a logical qubit. Therefore, after the main body of the syndrome measurement, a data qubit $data[i]$ of a logical qubit should be moved to its original location where it occupies in the logical qubit. Since, when the circuit synthesis is conducted for the syndrome measurement, the specific location of $data[i]$ is not determined yet, it is described symbolically as $data[i]^{init}$ (see Figure 8). In each SABRE iteration, an initial qubit mapping is randomly picked (see Figure 2), and therefore the initial position of $data[i]$ is determined at that time. Therefore, after picking a random initial qubit mapping, the instruction “*Move data[i] data[i]^{init}*” is translated to the instruction including a specific qubit index, for example “*Move data[i] 3*”. The circuit mapping algorithm then tries to move $data[i]$ from a current location to the physical qubit of index 3. Figure 9 shows the conceptual transformation of the protocol description during the circuit synthesis.

Sometimes, it may happen that the qubits already arrived at the designated positions may be moved to other places during treating the move of other qubits. When such a situation happens, we insert the *Move* about the qubit into FL forcibly and treat it again. Since the *Move-Back* is usually conducted at the last in the circuit, such forcible insertion into FL does not corrupt the logic of the circuit. If all the data qubits arrive at the target positions, the *Move-Back* for all the data qubits is completed.

We are now able to make a self-contained fault-tolerant quantum circuit for a single fault-tolerant quantum protocol. However, it is still not enough for universal fault-tolerant quantum computing yet. In the following subsection, we will see that which should be considered more for universal fault-tolerant quantum computing.

3.3 Circuits for universal fault-tolerant quantum computing

The third consideration for universal fault-tolerant quantum computing is that we need multiple fault-tolerant quantum computing protocols (and therefore circuits), for example, *H*, *T*, *CNOT*, *Encoder*,

and Measurement in the *Z* basis (*MeasZ*). All the protocols are differently designed for their own purpose but should act on the input having physically the same qubit arrangement, a logical qubit. For that, the circuit synthesis of each protocol has to share the position of data qubits of a logical qubit. Otherwise, if we focus on optimizing the circuit of each protocol separately, the initial qubit mapping for the circuit may be different from others, and therefore we need to perform the additional qubit movement conditioned on the situation (the last circuit and the next circuit).

To make all the circuits share the positions of the data qubits, we first need to make a reference initial qubit mapping for the protocols. For that, we first divide all the protocols into two categories, *pivot* protocols and *non-pivot* protocols, and perform the circuit mapping on the pivot protocols first. We then, in the circuit mapping on the non-pivot protocols, anchor the positions of the data qubits by following the results of the circuit mapping on pivot protocols when choosing a random initial mapping.

Then, with which criterion, the protocols can be categorized? As mentioned above, the circuit of a pivot protocol is generated from the scratch without any limitation on the qubit allocation and therefore it can be highly optimized by the circuit mapping method itself. But, the circuit of a non-pivot protocol is limited by the result of the pivot protocol. In this circumstance, for better performance, it is reasonable to choose the most frequently executed protocols as the pivot, and such protocol is, needless to say, the syndrome measurement. We therefore configure the logical qubit, the arrangement of physical qubits, from the initial qubit mapping of the circuit mapping on the syndrome measurement.

We first discuss 1-qubit logical operations: *Encoder*, *MeasZ*, and *H* gate. For the operations that can be implemented as transversal, the circuit mapping is very trivial. Therefore, here we discuss how to implement the fault-tolerant circuit about *Encoder*. Encoder is the operation that makes the quantum state of a logical qubit, a code block, to a logical zero state $|0\rangle_L$ or a logical plus state $|+\rangle_L$ where $|+\rangle_L = (|0\rangle_L + |1\rangle_L)/\sqrt{2}$. Before Encoder, all the component qubits of a logical qubit (or a code block) are not distinguished and have garbage quantum states. However, after *Encoder*, the data qubits of a logical qubit should be placed as determined in the circuit synthesis of the syndrome mea-

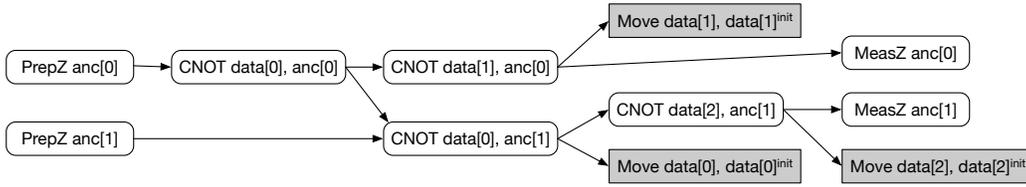


Figure 8: DAG of 3-qubit code syndrome measurement circuit. The *Move* instructions for all the data qubits are included at the last.

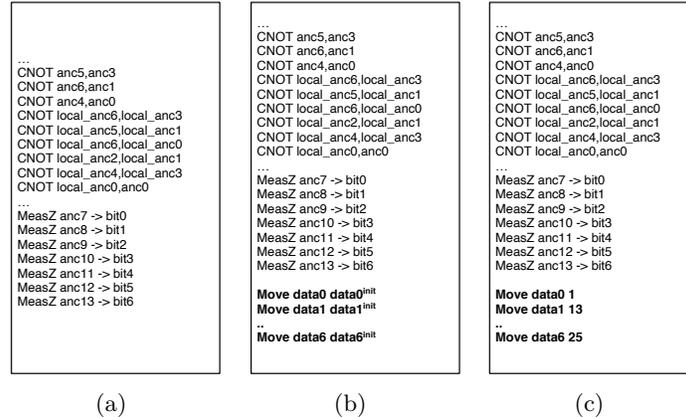


Figure 9: By adding the *Move* instruction, conceptually the QASM for the protocol is transformed from (a) \rightarrow (b) \rightarrow (c) during the circuit synthesis. (a) An example of a normal QASM, (b) The QASM with *Move* instruction with the symbolic representation of the initial position of the data qubits and (c) The QASM with a specific value of the initial position of the data qubits. As mentioned above, at the beginning of each SABRE iteration, the initial qubit mapping table is randomly generated. The specific initial position of the data qubits, e.g. as shown in the figure $\{\dots, data0^{init}: 1, data1^{init}: 13, \dots, data6^{init}: 25, \dots\}$, is determined from the qubit mapping table.

surement . See Figure 16 as an example. Therefore, after the main body of the *Encoder*, the *Move-Back* operation should be performed and the destination for each data qubit is, as mentioned above, specified from the configuration of a logical qubit not its initial position before *Encoder*.

For 2-qubit logical operations such as *CNOT* gate, the present work treats it as a protocol that acts on a single extended qubit layout. For example, suppose that a logical qubit is defined on the 2-dimensional rectangular qubit layout of size $m \times n$. We then extend the layout as $2m \times n$ for a vertical extension or $m \times 2n$ for a horizontal extension, and then allocate two logical qubits on it properly. Please see Figure 10. In doing so, all the physical operations for the 2-qubit logical operation act within two logical qubits. On the other hand, for reference, Ref. [3] uses the qubits outside the two logical qubits concerned as a communication channel.

A certain error-correcting code implements a logical *T* (and *S*) gate as a 2-qubit gate protocol acting

on a logical data qubit and a magic state (see Figure 11). In that case, the magic state preparation protocol (see Figure 13 of Ref. [10]) should be synthesized first and the fault-tolerant circuit of the *T* gate then is synthesized on the extended qubit layout. The layout extension is based on the qubit mappings of both the logical qubit and the magic state.

The logical *T* gate circuit can be synthesized in terms of two viewpoints, a combination of multiple basic quantum gates, and a single complex gate. The first is, as shown in Figure 11, we assemble the fault-tolerant circuits of logical *CNOT*, *MeasZ*, and *S* gates. For this, the magic (data) qubits of a magic state should be placed at the positions of the corresponding data qubits of a logical qubit to perform a logical *CNOT* gate. That is, the fault-tolerant circuit of a magic state preparation should include the *Move-Back* operation for the magic qubits with reference to the logical qubit. For that, the following instruction is required, *Move magic[i] destination[i]* where *destination[i]* corre-

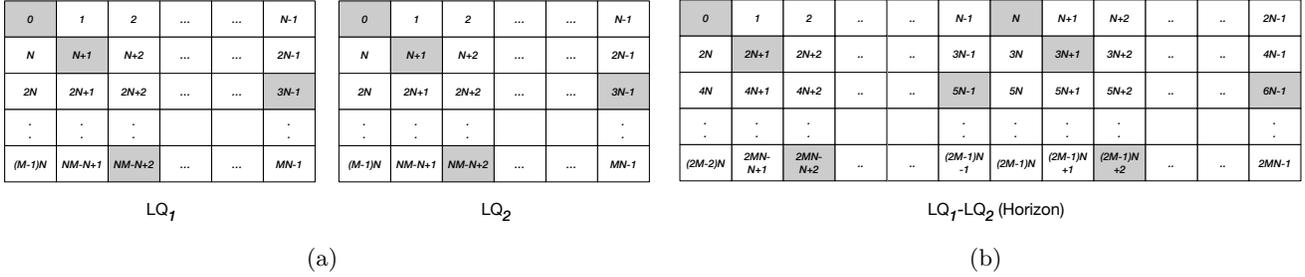


Figure 10: Example of the qubit layout extension. (a) Two copies of a single logical data block of the size $m \times n$, and (b) The horizontally extended qubit layout, of the size $m \times 2n$. The qubit layout can be extended in the vertical direction either. Gray cells indicate the data qubits in the logical qubit block. The physical index of each data qubit should be relabelled in the extended qubit layout.

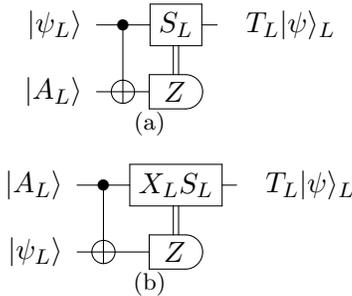


Figure 11: Logical T gate protocol that measures the magic state $|A\rangle_L$. S gate correction is required conditioned on the measurement outcome. (a) Protocol that measures the magic state, and (b) Protocol that measures the logical data qubit [11].

sponds to the index of the $data[i]$ of the logical qubit in the extended layout.

On the other hand, the circuit can be synthesized as a single complex gate either. In this case, unlike the first case, we don't need to consider the *Move-Back* in the magic state preparation because it is possible to make the circuit based on the mapping of magic qubits $magic[i]$ just after the main body of the preparation protocol. Besides, unlike the normal *CNOT* gate including the *Move-Back* of both the logical qubits, the magic qubits do not need to be back to the original position. Therefore, this synthesis requires fewer qubit movements than the first synthesis approach. To make a compact circuit, it is better to take the second approach. In this regard, we prefer the protocol in (a) of Figure 11 to (b) of the same figure. The *Move-Back* operation of the latter requires more *SWAP* gates than the former. Figure 13 shows the comparison between both approaches. Note that we applied this approach to the circuit synthesis for the magic

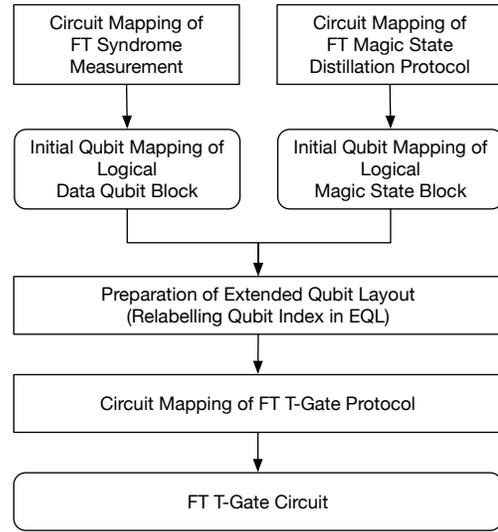


Figure 12: Flow of the circuit synthesis the logical T gate protocol. After mapping the pivot protocols (syndrome measurement and state distillation) respectively, it is possible to determine the extended qubit layout for the logical T gate protocol.

state preparation.

3.4 Circuit Partitioning

In general, in the circuit synthesis of an ordinary quantum algorithm, all the operations are placed as forward as possible to minimize the length of the circuit. However, to make an effective quantum circuit of a fault-tolerant protocol, we have to take its structure into account rather than unconditionally following the above-mentioned scheme.

A generic fault-tolerant quantum protocol begins by preparing ancilla qubits as a certain state and ends with the measurement of the ancilla qubits and the conditional processing based on the mea-

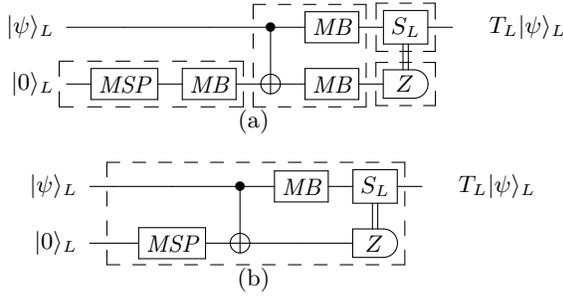


Figure 13: Comparison of the T circuits according to the synthesis approach. (a) the combination of basic gates. (b) single complex gate. Note that MSP and MB are respectively the abbreviations of the protocol of the magic state preparation and the Move-Back operation.

surement outcomes. In some cases, such a classical control operation is conducted once at the end of the protocol, but in other cases, performed multiple times within a single protocol. In the latter case, if the quantum circuit after the circuit synthesis has a properly partitioned form on the basis of the turn of classical processing, a classical controller can execute the protocol easily. Otherwise, the classical controller continuously needs to check the current progress of the circuit to find the turn for the classical control operations. In doing so, it may make a decision for delaying some quantum operations for synchronization on the fly. In what follows, we discuss how to make the quantum circuit of fault-tolerant quantum protocols partitioned without losing its logic.

For the circuit partitioning, we propose two techniques in this work. First, one introduces *barrier* statement [7] to the protocol and the circuit synthesis treats it. Second, one partitions the protocol beforehand, and performs the circuit synthesis individually but with sharing data common to all the tasks. By the way, since the second method is very trivial, we skip the detailed explanation here but will be demonstrated as an example in Section 6.

Suppose that the fault-tolerant protocol described in QASM includes the barrier statements at proper positions. Here, the proper position for the barrier statement is, on considering the structure of fault-tolerant quantum protocols, usually when just after all the ancilla qubits that were prepared within the protocol are measured. Please see Figures 3 and 15. Note that for the second method above we split the entire QASM up on the basis of the positions instead of inserting the *barrier* state-

ment.

Before going further, we need to say the following. Please remind that for finding a fault-tolerant qubit move path we trace the qubit usage status throughout a protocol. In this regard, the time when the usage status of all the ancilla qubits in the same category becomes *inactivated* is the above-mentioned proper position. Then, even without introducing the barrier statement, it is possible for the circuit synthesis algorithm to partition the circuit based on the usage status tracking. But, the present work does not keep this in mind because it may happen that the architect of a fault-tolerant quantum protocol may not want to split the circuit up. The circuit should work as the architect expects.

Back to the proposed method, let us say that the node including the barrier statement comes in FL after all of its preceding nodes are treated and exported to the quantum circuit. Please note that each node in DAG includes a quantum instruction (see Figure 8). If the barrier node is currently included in FL, we do not append the succeeding nodes (logically independent with the remaining nodes in FL) of the node just exported to a quantum circuit to FL, but keep them in a temporary list. If all the nodes except the barrier node are treated, that is, there remains only the barrier node in FL, all the nodes stored in the temporary list are moved to FL. After that, the barrier node is removed from FL. By doing so, the circuit can be logically partitioned. The circuit synthesis basically cannot do anything for the nodes coming after the barrier node before processing the barrier. Please see Figure 14 for the effect of the circuit partitioning. In (a) of the figure, both the quantum instructions belonging to before and after the barrier are mixed up at one time, but in (b) they are separated.

4 Example : Syndrome Measurement of $[[7, 1, 3]]$ Steane Code

We show the fault-tolerant quantum circuit for the stabilizer measurement of $[[7, 1, 3]]$ Steane code. We apply the Steane-EC method that consumes logical states $(|0\rangle_L, |+\rangle_L)$ of the code [9, 10, 12] (see Figure 3). The protocol is composed of the Z -stabilizer measure and the X -stabilizer measure in serial, and the Z (X)-stabilizer measure is composed of the preparation of the logical plus (zero) state, and a

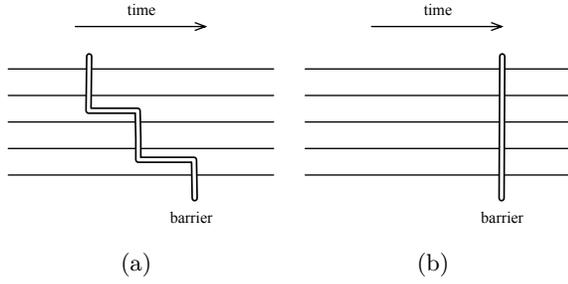


Figure 14: The effect of the circuit partitioning in the circuit synthesis for fault-tolerant quantum protocols. (a) Before the circuit partitioning, two sub-circuits that need to be separated in time are mixed in time flow. (b) Partitioned circuit.

sequence of *CNOT* gates between data qubits and the syndrome qubits. For the fault-tolerant preparation of a logical zero (plus) state, we apply Goto’s single ancilla qubit verification method [8] rather than the method comparing two copies of logical states [10]. In the method, a non-FT logical ancilla state is examined using a single checkup qubit. If the verification succeeds, the main body of the syndrome measurement begins. Otherwise, the logical ancilla state should be prepared again. But, we do not take the repetition caused by the non-deterministic feature into account throughout the present work because the purpose of the present work is to generate a fault-tolerant circuit.

Figure 15 shows the QASM of the protocol which includes the barrier statements. It is translated to DAG, and then the circuit synthesis is undergone. For the 2-dimensional qubit layout of size 5×7 , we have obtained a fault-tolerant quantum circuit of depth 35. Please see Figures 20~26. Each figure shows each part of the circuit: Preparation of $|+\rangle_L$, *CNOT* (*data*[*i*], *syndrome*[*i*]), Preparation of $|0\rangle_L$ and *CNOT* (*syndrome*[*i*], *data*[*i*]). The initial qubit mapping for the circuit is shown in Figure 16. Figure 27 shows the text representation of the circuit in JSON format, which is generated from our implementation of the circuit synthesis algorithm.

By processing the *barrier* statement, the entire circuit is separated into 4 sub-circuits in time flow even though it is not explicitly displayed there. Besides, by the *Move-Back* operation, it becomes that all the data qubits are placed at their initial positions after all the quantum operations. Please compare Figure 16 with Figure 26 (f).

```

PrepZ syndrome[0]
PrepZ syndrome[1]
PrepZ syndrome[2]
PrepZ syndrome[3]
PrepZ syndrome[4]
PrepZ syndrome[5]
PrepZ syndrome[6]
PrepZ checkup[0]
H syndrome[0]
H syndrome[4]
H syndrome[5]
H syndrome[6]
CNOT syndrome[0], syndrome[1]
CNOT syndrome[5], syndrome[3]
CNOT syndrome[6], syndrome[2]
CNOT syndrome[4], syndrome[1]
CNOT syndrome[0], syndrome[2]
CNOT syndrome[6], syndrome[3]
CNOT syndrome[5], syndrome[1]
CNOT syndrome[4], syndrome[6]
CNOT checkup[0], syndrome[0]
CNOT checkup[0], syndrome[5]
CNOT checkup[0], syndrome[6]
MeasZ checkup[0]
Barrier
CNOT data[0], syndrome[0]
CNOT data[1], syndrome[1]
CNOT data[2], syndrome[2]
CNOT data[3], syndrome[3]
CNOT data[4], syndrome[4]
CNOT data[5], syndrome[5]
CNOT data[6], syndrome[6]
MeasZ syndrome[0]
MeasZ syndrome[1]
MeasZ syndrome[2]
MeasZ syndrome[3]
MeasZ syndrome[4]
MeasZ syndrome[5]
MeasZ syndrome[6]
Barrier
PrepZ syndrome[0]
PrepZ syndrome[1]
PrepZ syndrome[2]
PrepZ syndrome[3]
PrepZ syndrome[4]
PrepZ syndrome[5]
PrepZ syndrome[6]
PrepZ checkup[0]
H syndrome[1]
H syndrome[2]
H syndrome[3]
H syndrome[4]
H syndrome[5]
H syndrome[6]
CNOT syndrome[1], syndrome[0]
CNOT syndrome[3], syndrome[5]
CNOT syndrome[2], syndrome[6]
CNOT syndrome[1], syndrome[4]
CNOT syndrome[2], syndrome[0]
CNOT syndrome[3], syndrome[6]
CNOT syndrome[1], syndrome[5]
CNOT syndrome[6], syndrome[4]
CNOT syndrome[5], checkup[0]
CNOT syndrome[6], checkup[0]
MeasZ checkup[0]
Barrier
CNOT syndrome[0], data[0]
CNOT syndrome[1], data[1]
CNOT syndrome[2], data[2]
CNOT syndrome[3], data[3]
CNOT syndrome[4], data[4]
CNOT syndrome[5], data[5]
CNOT syndrome[6], data[6]
H syndrome[0]
H syndrome[1]
H syndrome[2]
H syndrome[3]
H syndrome[4]
H syndrome[5]
H syndrome[6]
MeasZ syndrome[0]
MeasZ syndrome[1]
MeasZ syndrome[2]
MeasZ syndrome[3]
MeasZ syndrome[4]
MeasZ syndrome[5]
MeasZ syndrome[6]

```

Figure 15: QASM of the stabilizer measurement of $[[7, 1, 3]]$ Steane code [9, 10, 12]. Note that the declaration of qubits and classical bits are omitted. The Z (X)-type stabilizer measure is shown in the left (right) column. From the first line to the line just before the *barrier* statement the procedure of the logical ancilla state preparation (of Ref. [8]) is described, and the main procedure of the syndrome measure is shown thereafter.

5 Fault-Tolerant Circuits of $[[7, 1, 3]]$ Steane code FTQC

This section shows how to prepare a full set of fault-tolerant quantum circuits for $[[7, 1, 3]]$ Steane code-based fault-tolerant quantum computing. For that, we first need to determine which protocols are required and classify them into two categories, the *pivot* protocols and the *non-pivot* protocols. We then perform the circuit synthesis for the pivot protocols and apply their results to the circuit synthesis of the non-pivot protocols. Table 1 shows the protocols necessary for universal quantum computing divided into two categories.

data[5]	data[3]	syndrome[5]	dummy[5]	data[1]	data[0]	dummy[18]
dummy[13]	dummy[10]	syndrome[3]	dummy[6]	syndrome[1]	dummy[14]	data[2]
dummy[3]	dummy[2]	syndrome[6]	checkup[0]	syndrome[0]	dummy[17]	dummy[15]
data[6]	dummy[0]	syndrome[2]	dummy[7]	dummy[11]	syndrome[4]	dummy[19]
dummy[11]	dummy[16]	dummy[4]	dummy[8]	dummy[9]	dummy[12]	data[4]

Figure 16: The initial qubit mapping for the fault-tolerant circuit of the syndrome measurement which is shown continuously over Figure 20 ~ 26.

Table 1: Protocols for Steane code based universal FTQC

Type	Protocols
Pivot	Syndrome Measurement, Magic State Preparation
Non-Pivot	<i>PrepZ</i> (or <i>Encoder</i>), <i>MeasZ</i> , <i>H</i> , <i>T</i> , <i>S</i> , <i>CNOT</i>

Before proceeding to the circuit synthesis for the pivot protocols, let us discuss the qubit layout first. A qubit layout affects the cost and the performance of logical qubits, logical gates, and therefore, the entire quantum computing. Therefore we need to pay special attention to it. There exists an optimal qubit layout in terms of the circuit size defined as $\#qubit \times circuit_depth$, as the size of the layout increases the number of qubits is increasing but the circuit depth may be decreased until the lower bound. Therefore we need to compare the circuit sizes over various qubit layouts and select the best one. We then apply the chosen qubit layout to generate the set of full fault-tolerant quantum circuits in the following subsection.

5.1 Optimal Qubit Layout

Over 2-dimensional qubit layouts of size $5 \times 6 \sim 7 \times 8$, we quantify the size of the fault-tolerant quantum circuit for the syndrome measurement based on two error correction methods, Shor EC and Steane EC. For Steane EC [9, 10, 12], we exploit the fault-tolerant preparation of logical ancilla states $|0\rangle_L$ (and similarly $|+\rangle_L$) of Ref. [8] (see Figure 1 therein). For Shor EC [10, 12, 13], we apply the fault-tolerant preparation of the length-4 cat state described in Ref. [10] (see Figure 6 therein). To select the best qubit layout, we evaluate the circuits in terms of the circuit size, KQ [14], where *circuit size* is defined as $circuit_depth \times \#qubits$. We assume that in this work one ancilla state is generated in sequence, not multiple states in parallel.

Table 2 shows the circuit sizes of fault-tolerant syndrome measurements over the qubit layouts by adopting $\#gates$ and *circuit depth* as the performance evaluation criteria. It is well known that Shor-EC based protocol requires fewer qubits, but more quantum gates than Steane-EC based one [3, 10]. Therefore, for fault tolerance, the latter is preferred. As shown in the Table, our circuit synthesis results also show the same tendency. Based on the Table, we in the following section develop the circuits of fault-tolerant quantum protocols with the qubit layout of size 5×7 . For reference, in Ref. [3] the qubit layout of size 6×8 is applied to optimize the threshold than to optimize the space-time resource in the local setting.

Before going further, we emphasize again that since our proposed algorithm is heuristic and non-deterministic, the results the table shows are not fixed for the layout. They are just the most compact ones we have obtained so far, but there may exist more optimized circuits.

5.2 Full Set of Fault-Tolerant Quantum Circuits

We are going to perform the circuit mapping for the protocols listed in Table 1 in the following order. The first is the syndrome measurement and the magic state preparation in the pivot protocols. Since the fault-tolerant quantum circuit and the associated qubit mapping of the syndrome measurement are already described in Section 4, we discuss the magic state preparation only.

We take the protocol described in Ref. [10] (see Fig. 13 therein). It is composed of the repetition of the preparations of ancilla states (logical zero state and 7-qubit cat state), $\bar{T}\bar{X}\bar{T}^\dagger$ measurement and error detection. Since the ancilla preparations and error detection include the selection of the next operation conditioned on the measurement outcomes, we apply the circuit partitioning we have discussed before. For that, we insert the *barrier* statements in the protocol, a total of 10 times. The fault-tolerant preparations of a logical ancilla and a cat state respectively require a single checkup qubit. Therefore, by resuing qubits, the protocol is composed of at least 15 qubits: 7 for data, 7 for ancilla, and 1 for the verification. Finally, we emphasize that in the circuit synthesis of the magic state preparation (or distillation for other code), the final qubit mapping after the circuit execution is critical to the T gate

Table 2: The size of the fault-tolerant circuits about the syndrome measurement over various 2-dimensional qubit layouts. *ideal* indicates the static analysis about the the protocol itself. The number in parentheses indicates the number of qubits of the corresponding qubit layout. Note that the protocols based on Steane-EC and Shor-EC are composed of 15 and 12 qubits.

Method	item	<i>ideal</i>	5 × 6 (30)	5 × 7 (35)	6 × 6 (36)	5 × 8 (40)	6 × 7 (42)	6 × 8 (48)	7 × 7 (49)	7 × 8 (56)
Steane-EC	<i>depth</i>	18	43	35	41	40	41	41	40	38
	<i>#gates</i>	83	156	168	162	158	164	165	175	155
	<i>KQ</i>	270	1,290	1,225	1,476	1,600	1,722	1,968	1,960	2,128
Shor-EC	<i>depth</i>	44	55	53	54	55	53	55	52	54
	<i>#gates</i>	144	206	204	199	224	212	212	224	216
	<i>KQ</i>	528	1,650	1,855	1,944	2,200	2,226	2,640	2,548	3,025

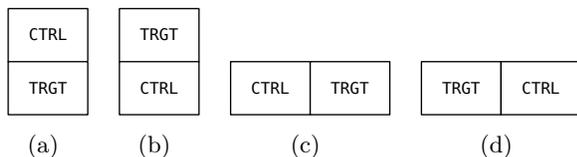


Figure 17: The relative arrangement of two logical qubits.

circuit.

We go to the non-pivot protocols. For the 1-qubit gate, only the circuit synthesis of the encoder is enough because the other gates can be implemented as the transversal gates, therefore there is nothing to do to realize a quantum circuit. As mentioned several times, we take the protocol for that consuming a single checkup qubit protocol [8]. Like the magic state, in the circuit of the encoder, the final qubit mapping is so important. It should be the configuration of the logical qubit. In the initial mapping of the encoder, all the qubits are just dummy qubits that do not hold any meaningful quantum state. The syndrome measurement and the magic state preparation include the encoder for the preparation of the logical ancilla qubits, but we don't apply the results there to the encoder and vice versa to make an optimized circuit for each respectively.

For the 2-qubit gates such as *CNOT* and *T*, we have to perform the circuit synthesis over all the cases of how two qubits are arranged on the logical qubit layout. Please see Figure 17. However, in the case of *CNOT*, all the data qubits in both logical qubits have to move back to their initial positions after the operation. Therefore, the circuits for the layouts (a) and (c) directly can be used for the layouts (b) and (d) by changing only the *CNOT* direc-

tions. On the other hand, for the *T* gate, as mentioned before, the *Move-Back* for the magic state is not required, and therefore the circuit for the layout (a) cannot be applied for the case (b). Similarly for the layouts (c) and (d). Therefore, we conduct the circuit synthesis of *T* gate over all four cases, but only two for *CNOT* gate. Figures 28 ~ 31 show all the snapshots of *CNOT* gate for the qubits arranged vertically, (*ctrl_n*, *trgt_s*), and Figures 32 ~ 38 show all the snapshots of *T* gate for the qubits arranged vertically, (*data_n*, *magic_s*).

To conclude this section, we list the setting and the result of the circuit synthesis over all the protocols shown in Table 1. Please see Table 3. Note that for the S gate correction in the T gate, we apply the transversal gate rather than the state injection method like the T gate protocol. For the fault tolerance, the state injection method is used but for the purpose of this work, the transversal gate is enough.

6 [[23, 1, 7]] Golay Code

[[23, 1, 7]] Golay code is well known as a high error correction threshold [10, 15], but it has been rarely studied how to realize universal fault-tolerant quantum computing with that code. Due to its large code block (logical qubit), it is a challenging problem to find fault-tolerant quantum circuits [16, 17].

It is also tricky and time-consuming to find the circuits with the proposed method. Therefore, in this work, we apply the *divide-and-conquer* approach to find the fault-tolerant quantum circuit of the syndrome measurement efficiently. That is, we divide the entire protocol into several sub-protocols, obtain the fault-tolerant circuit for each

Table 3: The static analysis of the fault-tolerant quantum circuits for universal fault-tolerant quantum computing. The numbers of *SWAP* gates and *Barrier* indicate the quantities of those ones introduced in the circuit synthesis. Note that the quantities of the other gates in the circuit are precisely the same as those included in the protocol. Note that MB indicates the Move-Back operation.

Operation	Protocol				Circuit			
	Reference	#Qubits	Depth	Gates	Depth	# <i>SWAP</i>	MB	#Barrier
Syndrome Measurement	[9, 10]	15	20	<i>CNOT</i> : 36, <i>H</i> : 15, <i>PrepZ</i> : 16, <i>MeasZ</i> : 16	35	80	O	3
Encoder	[8]	8	8	<i>CNOT</i> : 11, <i>H</i> : 3, <i>PrepZ</i> : 8, <i>MeasZ</i> : 1	18	31	O	-
Magic State Preparation	[10]	15	75	<i>CNOT</i> : 113, <i>H</i> : 49, <i>PepZ</i> : 49, <i>MeasZ</i> : 49, <i>T</i> : 14, <i>T</i> [†] : 14	162	323	X	10
h- <i>CNOT</i>	Transversal	14	1	<i>CNOT</i> : 7	21	136	O	-
v- <i>CNOT</i>	Transversal	14	1	<i>CNOT</i> : 7	13	80	O	-
h- <i>T</i> (d_e, m_w)	Figure 13 (b)	14	3	<i>CNOT</i> : 7, <i>MeasZ</i> : 7, <i>S</i> : 7	22	96	O	1
h- <i>T</i> (d_w, m_e)	Figure 13 (b)	14	3	<i>CNOT</i> : 7, <i>MeasZ</i> : 7, <i>S</i> : 7	20	104	O	1
v- <i>T</i> (d_n, m_s)	Figure 13 (b)	14	3	<i>CNOT</i> : 7, <i>MeasZ</i> : 7, <i>S</i> : 7	17	71	O	1
v- <i>T</i> (d_s, m_n)	Figure 13 (b)	14	3	<i>CNOT</i> : 7, <i>MeasZ</i> : 7, <i>S</i> : 7	24	81	O	1

sub-protocol by applying the proposed algorithm, and finally combine all the sub-circuits. We hire the protocol of preparing a logical zero state of Ref. [16], and divide it into the non-FT preparation stage of $|0\rangle_L$ and the verification stage (see Figures 3 and 4 therein). We then perform the circuit synthesis of the former and apply the result to the synthesis of the latter. Please note that the fact that the former acts in a non-fault-tolerant manner does not indicate that its non-FT circuit is enough for that. By taking the divide-and-conquer method, the entire circuit can be naturally partitioned, and classical control operations can be conducted between the sub-circuits.

Let us assume that the size of the qubit layout for the above non-FT preparation circuit is $m \times n$. Then for the fault-tolerant circuit for the verification part, we need an extended qubit layout of size $2m \times 2n$ (see Figure 19). The initial qubit mapping is constituted of 4 copies of the final mapping of the non-FT preparation circuit (see Figure 18). How to extend qubit layout was discussed in Section 3.3. We then apply the circuit synthesis algorithm to find the fault-tolerant circuit functioning for the verification, and then combine the resulting circuit with four copies of the non-FT circuit for preparing $|0\rangle_L$. We now have a fault-tolerant circuit for the preparation of a logical zero state. Since the code is self-dual, the fault-tolerant circuit for the preparation of $|+\rangle_L$ is almost the same as the FT circuit for preparing $|0\rangle_L$.

For [[7, 1, 3]] Steane code FTQC, we determined

data[3]				data[12]	data[8]	data[16]
	data[1]		data[18]			
data[15]	data[20]	data[22]	data[11]	data[5]	data[21]	
data[13]	data[6]	data[4]			data[9]	
			data[7]	data[17]		data[0]
			data[14]		data[19]	data[2]
	data[10]					

Figure 18: Qubit layout of size 7×7 for a logical zero state $|0\rangle_L$ in [[23, 1, 7]] Golay code of Ref. [16]. Based on this layout of 49 qubits, we obtain a fault-tolerant circuit of the preparation protocol (Figure 4 therein). The circuit includes 269 *SWAP* gates to make 57 *CNOT* gates executable on the qubit layout without noisy *SWAP* gates between data qubits. Empty cells indicate dummy qubits working as the communication channels.

the configuration of a logical qubit from the circuit synthesis result of the syndrome measurement protocol. We applied the Steane-EC method that requires logical states $|0\rangle_L$ and $|+\rangle_L$ as ancilla states. For the fault-tolerant preparation of logical states, we refer to Ref. [8] that is composed of the non-FT preparation of one logical state and the verification of it by use of 1 physical qubit. For the Golay code, we take the same approach, but the difference is the complexity of the fault-tolerant preparation of logical states as mentioned above. We can say that the non-FT preparation of logical states $|0\rangle_L$ and $|+\rangle_L$ is the dominant part of the syndrome measurement protocol in the Golay code QEC. There-

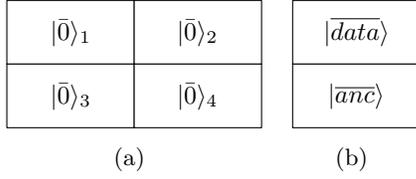


Figure 19: Qubit Layouts for $[[23, 1, 7]]$ Golay code. (a) Extended qubit layout for encoding $|0\rangle_L$ in the fault-tolerant manner [16] (see Figure 3 therein). Each cell, shown in Figure 18, indicates the code block for the corresponding logical zero state $|\bar{0}\rangle_i$ prepared in the non-fault-tolerant manner. (b) Extended qubit layout for a logical qubit composed of the code blocks of data qubits $|\overline{data}\rangle$ and logical ancilla $|\overline{anc}\rangle$. Each cell is arranged as the code block shown in Figure 18, but the roles of the qubits in the block differ.

fore, in this work, we determine the configuration of a logical qubit from the circuit synthesis of the non-FT preparation protocol.

As mentioned several times, the fault-tolerant preparation of the logical states in the Golay code takes much time and space (qubits). In this work, we assume logical ancilla states are supplied from an ancilla factory, not generated at site. Therefore, with the 2-dimensional qubit layout of size 14×7 , we define a logical qubit made of the 23 data qubits, the 23 ancilla qubits for a logical ancilla state, and some dummy qubits for the communication channel. We leave a detailed method about how to supply the logical ancilla states practically as future work.

The code distance of the Golay code is 7 and therefore it is possible to correct arbitrary 3-qubit errors. Therefore, as mentioned above, it is possible to allow a one-time noisy *SWAP* gate between data-type qubits during the syndrome measurement, $\lfloor (7-1)/4 \rfloor = 1$. Please note that in the fault-tolerant preparation of logical ancilla states, we do not permit any noisy *SWAP* gate between the data-type qubits. Table 4 describes the procedure and the static data of the circuit synthesis of the fault-tolerant preparation of the logical zero states and the syndrome measurement.

7 Discussion

We leave some comments for the readers who are going to implement our algorithm or develop new ones.

The circuit synthesis for an ordinary quantum al-

gorithm always succeeds in finding a quantum circuit if the size of a quantum chip (qubit layout) is not less than the number of qubits in the quantum algorithm. According to a target case (quantum algorithm, qubit connectivity, and an initial qubit mapping), the quality of the resulting circuit or the efficiency of the synthesis procedure may be very poor, but nothing makes the circuit mapping impossible fundamentally.

On the other hand, for a fault-tolerant quantum protocol, the situation differs because in the circuit the qubits have to move in a fault-tolerant manner. If the size of a target quantum chip equals to or is bigger modestly than the number of qubits in the fault-tolerant protocol, the circuit synthesis may fail to find a fault-tolerant circuit. Particularly, the proposed algorithm tries to find a fault-tolerant quantum circuit based on a randomly picked initial qubit mapping, such a phenomenon that a circuit algorithm cannot generate a fault-tolerant circuit happens more frequently when the size of the quantum chip is not greater remarkably. In our implementation, we apply the time limit for SABRE traversal, the amount of which is proportional to the size of the protocol. If the SABRE iteration is not completed within the time limit, we forcibly turn off the current SABRE iteration and begin the next iteration.

In the present work, we have not discussed a lower bound on the size of a quantum chip for an n -qubit fault-tolerant quantum protocol. Finding such a bound theoretically is combinatorially extremely challenging. It depends on the initial qubit mapping, the property of a quantum protocol (highly parallel or serial), the shape of the qubit layout, and so on. For the purpose of reference, we have observed that for the Steane-EC based syndrome measurement protocol the proposed algorithm succeeds in finding a fault-tolerant quantum circuit acting on the qubit layout of 4×5 , but of longer depth 72. Since the protocol itself is designed as using 15 qubits, the minimum requirement for the fault-tolerant communication may not be so large but at cost of the circuit depth.

The proposed algorithm continuously selects a locally optimal *SWAP* gate. In that case, even though a selected *SWAP* gate was evaluated as optimal at a cost evaluation at the time, it may not play a significant role in the resulting circuit finally. For example, it may happen that occasionally con-

Table 4: Process and static analysis for the circuit synthesis of $[[23, 1, 7]]$ Golay code. The entire circuit synthesis is undergone in sequence: 1) Non-FT preparation of $|0\rangle_L (|+\rangle_L)$, 2) Verification and 3) Syndrome Measurement. Note that *Move-Back** is a partial move-back operation for the data qubits in $|\bar{0}\rangle_1$, not for all. Note that the value in parentheses in Circuit Depth indicates the circuit depth at the protocol level without the locality effect of the qubit layout. The circuit depth includes the physical preparation of $|0\rangle$.

	Protocol		
	Non-FT preparation of $ 0\rangle_L (+\rangle_L)$	Verification	Syndrome Measurement
Qubit Mapping	$M_{init} \rightarrow \dots \rightarrow M_{LQ}$	$M_{LQ} \rightarrow \dots \rightarrow M_{LQ}$ (<i>Move-Back*</i>)	$M_{LQ} \rightarrow \dots \rightarrow M_{LQ}$ (<i>Move-Back</i>)
Size of Qubit Layout	$m \times n$	$2m \times 2n$	$2m \times n$ (or $m \times 2n$)
Allowable Noisy <i>SWAP</i> between Data Qubits	0	0	1
Circuit Depth (Ideal Depth)	51 (9)	21 (4)	11 (5)
# <i>SWAP</i>	269	296	50

secutive *SWAP* gates for a pair of qubits are involved in the circuit. In this work, even though we have not represented it explicitly, we deal with the problem in two stages. First, during the circuit mapping, if a selected *SWAP* gate at the current cost evaluation is the same as the previous one, then we reject the selection and take a random one. Please note that here the selected *SWAP* gate should work on a pair of a data-type qubit and a non-data-type qubit in general. Otherwise, we refuse to take it. Second, after each SABRE iteration, as post-processing for the resulting circuit, we cancel out the quantum instructions repeated consecutively on the same qubits.

We now discuss future works caused by our report. This work defines the qubit configuration of a logical qubit from the circuit synthesis of the syndrome measurement, and then obtain compact fault-tolerant quantum circuits based on that configuration. For the 2-qubit gates, we have considered all the possible relative arrangements of logical qubits. As shown in Table 3, the sizes of the circuits are different according to the arrangement. This is because both the layout for a logical qubit and the arrangement of physical qubits in the logical qubit are not symmetric. Even though an individual quantum circuit is optimized in terms of the circuit depth, operating universal fault-tolerant quantum computing may be tricky because according to the qubit arrangement *CNOT* (*T*) gate works differently. In this regard, we need to consider how to operate universal fault-tolerant quantum computing efficiently with the quantum circuits of non-uniform performance.

8 Conclusion

We summarize the present work. To date, various concatenated quantum codes and their fault-tolerant protocols have been proposed theoretically, but their realization in the local setting has been rarely discussed. Only for a few well-known codes, their fault-tolerant circuits obtained by hand works have been reported. Those results or methodologies can not be directly applied to different qubit layouts or concatenated quantum codes.

In the present work, to automate the fault-tolerant quantum circuit synthesis, we raised four requirements, presented our approaches for them, and described how to implement them with the existing heuristic quantum circuit mapping algorithm. As a result, it is now possible to obtain a set of fault-tolerant quantum circuits for an arbitrary concatenated quantum code by running the algorithm.

The proposed algorithm does not work deterministically, and therefore the presented static analysis data about the circuits are not fixed for the protocol and the qubit layout. To get the most optimized circuits, we need to iterate the synthesis (SABRE) rounds as much as possible.

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data[5]	data[3]	syndrome[5]	dummy[5]	data[1]	data[0]	dummy[18]
dummy[13]	dummy[10]	syndrome[3]	dummy[6]	syndrome[1]	dummy[14]	data[2]
dummy[3]	dummy[2]	syndrome[6]	checkup[0]	syndrome[0]	dummy[17]	dummy[15]
data[6]	dummy[0]	syndrome[2]	dummy[7]	dummy[1]	syndrome[4]	dummy[19]
dummy[11]	dummy[16]	dummy[4]	dummy[8]	dummy[9]	dummy[12]	data[4]

(a) Step 1

data[5]	data[3]	syndrome[5]	dummy[5]	data[1]	dummy[18]	data[0]
dummy[13]	dummy[10]	syndrome[3]	dummy[6]	syndrome[1]	dummy[14]	dummy[15]
dummy[3]	dummy[2]	syndrome[6]	checkup[0]	syndrome[0]	dummy[17]	data[2]
dummy[0]	data[6]	syndrome[2]	dummy[7]	dummy[1]	syndrome[4]	dummy[19]
dummy[11]	dummy[16]	dummy[4]	dummy[8]	dummy[9]	data[4]	dummy[12]

(b) Step 2

data[5]	data[3]	syndrome[5]	dummy[5]	dummy[18]	data[1]	data[0]
dummy[13]	dummy[10]	syndrome[3]	dummy[6]	syndrome[1]	dummy[14]	dummy[15]
dummy[3]	dummy[2]	syndrome[6]	checkup[0]	syndrome[0]	dummy[17]	dummy[19]
dummy[0]	data[6]	syndrome[2]	dummy[7]	dummy[1]	syndrome[4]	data[2]
dummy[11]	dummy[16]	dummy[4]	dummy[8]	data[4]	dummy[9]	dummy[12]

(c) Step 3

data[5]	data[3]	syndrome[5]	dummy[5]	dummy[18]	data[1]	data[0]
dummy[13]	dummy[10]	syndrome[3]	dummy[6]	syndrome[1]	dummy[14]	dummy[15]
dummy[3]	dummy[2]	syndrome[6]	checkup[0]	syndrome[0]	syndrome[4]	dummy[19]
dummy[0]	data[6]	syndrome[2]	dummy[7]	dummy[1]	dummy[17]	data[2]
dummy[11]	dummy[16]	dummy[4]	dummy[8]	data[4]	dummy[9]	dummy[12]

(d) Step 4

data[5]	data[3]	syndrome[5]	dummy[5]	dummy[18]	data[1]	data[0]
dummy[13]	dummy[10]	syndrome[3]	dummy[6]	dummy[14]	syndrome[1]	dummy[15]
dummy[3]	dummy[2]	syndrome[6]	checkup[0]	dummy[1]	syndrome[4]	dummy[19]
dummy[0]	data[6]	dummy[7]	syndrome[2]	syndrome[0]	dummy[17]	data[2]
dummy[11]	dummy[16]	dummy[4]	dummy[8]	data[4]	dummy[9]	dummy[12]

(e) Step 5

data[5]	data[3]	syndrome[5]	dummy[5]	dummy[18]	data[1]	data[0]
dummy[13]	syndrome[3]	dummy[10]	dummy[6]	dummy[14]	syndrome[1]	dummy[15]
dummy[3]	dummy[2]	dummy[7]	checkup[0]	dummy[1]	syndrome[4]	dummy[19]
dummy[0]	data[6]	syndrome[6]	syndrome[2]	syndrome[0]	dummy[17]	data[2]
dummy[11]	dummy[16]	dummy[4]	dummy[8]	data[4]	dummy[9]	dummy[12]

(f) Step 6

Figure 20: The first part of the fault-tolerant quantum circuit of stabilizer measurement of $[[7, 1, 3]]$ Steane code: Fault-tolerant preparation of the logical state $|+\rangle_L$. Note that the rectangles, rounded rectangles, hexagons and bi-directed arrow respectively indicate H , $PrepZ$, $MeasZ$ and $SWAP$ gates.

data[5]	data[3]	dummy[10]	dummy[5]	dummy[18]	data[1]	data[0]
syndrome[3]	dummy[13]	syndrome[5]	dummy[6] ↔ syndrome[1]	dummy[14]	dummy[15]	
dummy[3]	dummy[2]	dummy[7]	checkup[0] • ⊕	syndrome[0]	dummy[17]	dummy[19]
dummy[0]	data[6]	syndrome[6]	dummy[8]	dummy[1] ↔ syndrome[4]	data[2]	
dummy[11]	dummy[16]	dummy[4]	syndrome[2]	data[4]	dummy[9]	dummy[12]

(a) Step 7

data[5]	data[3]	dummy[10]	dummy[5]	dummy[18]	data[1]	data[0]
syndrome[3]	dummy[13]	syndrome[5] • ⊕	syndrome[1]	dummy[6]	dummy[14]	dummy[15]
dummy[3]	dummy[2]	dummy[7]	← checkup[0]	syndrome[0]	dummy[17]	dummy[19]
dummy[0]	data[6]	syndrome[6]	dummy[8]	← syndrome[4]	dummy[1]	data[2]
dummy[11]	dummy[16]	dummy[4]	syndrome[2]	data[4]	dummy[9]	dummy[12]

(b) Step 8

data[5]	data[3]	dummy[10]	dummy[5]	dummy[18]	data[1]	data[0]
syndrome[3]	dummy[13]	syndrome[5]	• ⊕	syndrome[1]	dummy[6]	dummy[15]
dummy[3]	dummy[2]	checkup[0] • ⊕	• ⊕	syndrome[0]	dummy[17]	dummy[19]
dummy[0]	data[6]	syndrome[6] • ⊕	• ⊕	syndrome[4]	dummy[8]	data[2]
dummy[11]	dummy[16]	dummy[4]	syndrome[2]	data[4]	dummy[9]	dummy[12]

(c) Step 9

data[5]	data[3]	dummy[10]	dummy[5]	dummy[18]	data[1]	data[0]
syndrome[3]	dummy[13]	syndrome[5]	• ⊕	syndrome[1]	dummy[6]	dummy[15]
dummy[3]	dummy[2]	checkup[0] • ⊕	• ⊕	syndrome[0]	dummy[17]	dummy[19]
dummy[0]	data[6]	syndrome[6] • ⊕	• ⊕	syndrome[4]	dummy[8]	data[2]
dummy[11]	dummy[16]	dummy[4]	syndrome[2]	data[4]	dummy[9]	dummy[12]

(d) Step 10

data[5]	data[3]	dummy[10]	dummy[5]	dummy[18]	data[1]	data[0]
syndrome[3]	dummy[13]	syndrome[5]	• ⊕	syndrome[1]	dummy[6]	dummy[15]
dummy[3]	dummy[2]	checkup[0] • ⊕	• ⊕	syndrome[0]	dummy[17]	dummy[19]
dummy[0]	data[6]	syndrome[6] • ⊕	• ⊕	syndrome[4]	dummy[8]	data[2]
dummy[11]	dummy[16]	dummy[4]	syndrome[2]	data[4]	dummy[9]	dummy[12]

(e) Step 11

data[5]	data[3]	dummy[10]	dummy[5]	dummy[18]	data[1]	data[0]
syndrome[3]	dummy[13]	syndrome[5]	• ⊕	syndrome[1]	dummy[6]	dummy[15]
dummy[3]	dummy[2]	<checkup[0]>	• ⊕	syndrome[0]	dummy[17]	dummy[19]
dummy[0]	data[6]	syndrome[6]	• ⊕	syndrome[4]	dummy[8]	data[2]
dummy[11]	dummy[16]	dummy[4]	syndrome[2]	data[4]	dummy[9]	dummy[12]

(f) Step 12 (Barrier)

Figure 21: (Continued from Figure 20) The first part of the fault-tolerant quantum circuit of stabilizer measurement of $[[7, 1, 3]]$ Steane code: Fault-tolerant preparation of the logical state $|+\rangle_L$. Note that the rectangles, rounded rectangles, hexagons and bi-directed arrow respectively indicate H , $PrepZ$, $MeasZ$ and $SWAP$ gates.

data[5]	data[3]	dummy[10]	dummy[5]	dummy[18]	data[1]	data[0]
syndrome[3]	dummy[13]	syndrome[5]	syndrome[1]	dummy[6]	dummy[14]	dummy[15]
dummy[3]	dummy[2]	checkup[0]	dummy[7]	syndrome[0]	dummy[17]	dummy[19]
dummy[0]	data[6]	syndrome[6]	syndrome[4]	dummy[8]	dummy[1]	data[2]
dummy[11]	dummy[16]	dummy[4]	syndrome[2]	data[4]	dummy[9]	dummy[12]

(a) Step 13

data[5]	dummy[13]	dummy[10]	dummy[5]	data[1]	dummy[18]	dummy[15]
syndrome[3]	data[3]	syndrome[5]	syndrome[1]	dummy[6]	dummy[14]	data[0]
dummy[3]	dummy[2]	checkup[0]	dummy[7]	dummy[17]	syndrome[0]	dummy[19]
dummy[0]	data[6]	<syndrome[6]>	syndrome[4]	data[4]	dummy[1]	dummy[12]
dummy[11]	dummy[16]	dummy[4]	syndrome[2]	dummy[8]	dummy[9]	data[2]

(b) Step 14

dummy[13]	data[5]	dummy[10]	data[1]	dummy[5]	dummy[18]	dummy[15]
<syndrome[3]>	data[3]	syndrome[5]	syndrome[1]	dummy[6]	data[0]	dummy[14]
dummy[3]	dummy[2]	checkup[0]	dummy[7]	dummy[17]	syndrome[0]	dummy[19]
dummy[0]	data[6]	syndrome[6]	<syndrome[4]>	data[4]	dummy[1]	dummy[12]
dummy[11]	dummy[16]	dummy[4]	dummy[8]	syndrome[2]	dummy[9]	data[2]

(c) Step 15

dummy[13]	dummy[10]	data[5]	data[1]	dummy[5]	dummy[18]	dummy[15]
syndrome[3]	data[3]	syndrome[5]	<syndrome[1]>	dummy[6]	data[0]	dummy[14]
dummy[3]	dummy[2]	checkup[0]	dummy[7]	dummy[17]	<syndrome[0]>	dummy[19]
dummy[0]	data[6]	syndrome[6]	syndrome[4]	data[4]	dummy[1]	dummy[12]
dummy[11]	dummy[16]	dummy[4]	dummy[8]	dummy[9]	syndrome[2]	data[2]

(d) Step 16

dummy[13]	dummy[10]	data[5]	data[1]	dummy[5]	dummy[18]	dummy[15]
syndrome[3]	data[3]	<syndrome[5]>	syndrome[1]	dummy[6]	data[0]	dummy[14]
dummy[3]	dummy[2]	checkup[0]	dummy[7]	dummy[17]	syndrome[0]	dummy[19]
dummy[0]	data[6]	syndrome[6]	syndrome[4]	data[4]	dummy[1]	dummy[12]
dummy[11]	dummy[16]	dummy[4]	dummy[8]	dummy[9]	<syndrome[2]>	data[2]

(e) Step 17 (Barrier)

Figure 22: The second part of the fault-tolerant quantum circuit of stabilizer measurement of $[[7, 1, 3]]$ Steane code: Transversal $CNOT$ between data qubits and syndrome qubits. Note that the rectangles, rounded rectangles, hexagons and bi-directed arrow respectively indicate H , $PrepZ$, $MeasZ$ and $SWAP$ gates.

dummy [13]	dummy [10]	data [5]	data [1]	dummy [5]	dummy [18]	dummy [15]
syndrome [3]	data [3]	syndrome [5]	syndrome [1]	dummy [6]	data [0]	dummy [14]
dummy [3]	dummy [2]	checksum [0]	dummy [7]	dummy [17]	syndrome [0]	dummy [19]
dummy [0]	data [6]	syndrome [6]	syndrome [4]	data [4]	dummy [1]	dummy [12]
dummy [11]	dummy [16]	dummy [4]	dummy [8]	dummy [9]	syndrome [2]	data [2]

(a) Step 18

dummy [13]	data [5]	dummy [10]	data [1]	dummy [5]	dummy [18]	dummy [15]
syndrome [3]	dummy [2]	syndrome [5]	syndrome [1]	dummy [6]	data [0]	dummy [14]
dummy [3]	data [3]	checksum [0]	dummy [7]	dummy [17]	syndrome [0]	dummy [19]
data [6]	dummy [0]	syndrome [6]	syndrome [4]	dummy [1]	data [4]	data [2]
dummy [11]	dummy [16]	dummy [4]	dummy [8]	dummy [9]	syndrome [2]	dummy [12]

(b) Step 19

dummy [13]	data [5]	dummy [10]	data [1]	dummy [5]	dummy [18]	dummy [15]
syndrome [3]	syndrome [5]	dummy [2]	syndrome [1]	dummy [6]	data [0]	dummy [14]
dummy [3]	data [3]	checksum [0]	dummy [7]	syndrome [0]	dummy [17]	dummy [19]
dummy [11]	dummy [0]	dummy [4]	syndrome [4]	dummy [1]	data [4]	data [2]
data [6]	dummy [16]	syndrome [6]	dummy [8]	dummy [9]	syndrome [2]	dummy [12]

(c) Step 20

dummy [13]	data [5]	dummy [10]	data [1]	dummy [5]	dummy [18]	dummy [15]
syndrome [3]	syndrome [5]	dummy [2]	dummy [7]	dummy [6]	data [0]	dummy [14]
dummy [3]	data [3]	checksum [0]	syndrome [1]	syndrome [0]	dummy [17]	dummy [19]
dummy [11]	dummy [0]	dummy [4]	syndrome [4]	dummy [1]	data [4]	data [2]
data [6]	dummy [16]	dummy [8]	syndrome [6]	syndrome [2]	dummy [9]	dummy [12]

(d) Step 21

dummy [13]	data [5]	dummy [10]	data [1]	dummy [5]	dummy [18]	dummy [15]
dummy [3]	dummy [2]	syndrome [5]	dummy [7]	dummy [6]	data [0]	dummy [14]
syndrome [3]	data [3]	checksum [0]	syndrome [1]	syndrome [0]	dummy [17]	dummy [19]
dummy [11]	dummy [0]	dummy [4]	syndrome [4]	dummy [1]	dummy [9]	data [2]
data [6]	dummy [16]	dummy [8]	syndrome [6]	syndrome [2]	data [4]	dummy [12]

(e) Step 22

dummy [13]	data [5]	dummy [10]	data [1]	dummy [5]	dummy [18]	dummy [15]
dummy [3]	dummy [2]	syndrome [5]	dummy [7]	dummy [6]	data [0]	dummy [14]
dummy [11]	data [3]	checksum [0]	syndrome [1]	dummy [1]	dummy [17]	dummy [19]
syndrome [3]	dummy [0]	dummy [4]	syndrome [4]	syndrome [0]	dummy [9]	data [2]
data [6]	dummy [16]	syndrome [6]	dummy [8]	syndrome [2]	data [4]	dummy [12]

(f) Step 23

Figure 23: The third part of the fault-tolerant quantum circuit of stabilizer measurement of $[[7, 1, 3]]$ Steane code: Fault-tolerant preparation of the logical state $|0\rangle_L$. Note that the rectangles, rounded rectangles, hexagons and bi-directed arrow respectively indicate H , $PrepZ$, $MeasZ$ and $SWAP$ gates.

dummy [13]	data [5]	dummy [10]	data [1]	dummy [5]	dummy [18]	dummy [15]
dummy [3]	dummy [2]	syndrome [5]	syndrome [1]	dummy [6]	data [0]	dummy [14]
dummy [11]	data [3]	checkup [0]	dummy [7]	dummy [1]	dummy [17]	dummy [19]
dummy [0]	syndrome [3]	syndrome [4]	dummy [4]	syndrome [0]	dummy [9]	data [2]
data [6]	syndrome [6]	dummy [16]	dummy [8]	syndrome [2]	data [4]	dummy [12]

(a) Step 24

dummy [13]	data [5]	dummy [10]	data [1]	dummy [5]	dummy [18]	dummy [15]
dummy [3]	dummy [2]	syndrome [5]	syndrome [1]	dummy [6]	data [0]	dummy [14]
dummy [11]	data [3]	dummy [7]	checkup [0]	syndrome [0]	dummy [17]	dummy [19]
dummy [0]	syndrome [3]	dummy [16]	dummy [4]	dummy [1]	dummy [9]	data [2]
data [6]	syndrome [6]	syndrome [4]	dummy [8]	syndrome [2]	data [4]	dummy [12]

(b) Step 25

dummy [13]	data [5]	dummy [10]	data [1]	dummy [5]	dummy [18]	dummy [15]
dummy [3]	dummy [2]	syndrome [5]	syndrome [1]	dummy [6]	data [0]	dummy [14]
dummy [11]	data [3]	dummy [7]	checkup [0]	syndrome [0]	dummy [17]	dummy [19]
dummy [0]	syndrome [3]	dummy [16]	dummy [4]	dummy [1]	dummy [9]	data [2]
data [6]	syndrome [6]	syndrome [4]	dummy [8]	syndrome [2]	data [4]	dummy [12]

(c) Step 26

dummy [13]	data [5]	dummy [10]	data [1]	dummy [5]	dummy [18]	dummy [15]
dummy [3]	dummy [2]	syndrome [5]	syndrome [1]	dummy [6]	data [0]	dummy [14]
dummy [11]	data [3]	checkup [0]	dummy [7]	syndrome [0]	dummy [17]	dummy [19]
dummy [0]	syndrome [3]	dummy [16]	dummy [4]	dummy [1]	dummy [9]	data [2]
data [6]	syndrome [6]	dummy [8]	syndrome [4]	syndrome [2]	data [4]	dummy [12]

(d) Step 27

dummy [13]	data [5]	dummy [10]	data [1]	dummy [5]	dummy [18]	dummy [15]
dummy [3]	dummy [2]	syndrome [5]	syndrome [1]	dummy [6]	data [0]	dummy [14]
dummy [11]	data [3]	checkup [0]	dummy [7]	syndrome [0]	dummy [17]	dummy [19]
dummy [0]	syndrome [3]	dummy [16]	dummy [4]	dummy [1]	dummy [9]	data [2]
data [6]	dummy [8]	syndrome [6]	syndrome [4]	syndrome [2]	data [4]	dummy [12]

(e) Step 28

dummy [13]	data [5]	dummy [10]	data [1]	dummy [5]	dummy [18]	dummy [15]
dummy [3]	dummy [2]	syndrome [5]	syndrome [1]	dummy [6]	data [0]	dummy [14]
dummy [11]	data [3]	dummy [16]	dummy [7]	syndrome [0]	dummy [17]	dummy [19]
dummy [0]	syndrome [3]	checkup [0]	dummy [4]	dummy [1]	dummy [9]	data [2]
data [6]	dummy [8]	syndrome [6]	syndrome [4]	syndrome [2]	data [4]	dummy [12]

(f) Step 29

Figure 24: (Continued from Figure 23) The third part of the fault-tolerant quantum circuit of stabilizer measurement of $[[7, 1, 3]]$ Steane code: Fault-tolerant preparation of the logical state $|0\rangle_L$. Note that the rectangles, rounded rectangles, hexagons and bi-directed arrow respectively indicate H , $PrepZ$, $MeasZ$ and $SWAP$ gates.

dummy [13]	data [5]	dummy [10]	data [1]	dummy [5]	dummy [18]	dummy [15]
dummy [3]	dummy [2]	syndrome [5]	syndrome [1]	dummy [6]	data [0]	dummy [14]
dummy [11]	data [3]	dummy [16]	dummy [7]	syndrome [0]	dummy [17]	dummy [19]
dummy [0]	syndrome [3]	<checkup [0]>	dummy [4]	dummy [1]	dummy [9]	data [2]
data [6]	dummy [8]	syndrome [6]	syndrome [4]	syndrome [2]	data [4]	dummy [12]

(a) Step 30 (Barrier)

Figure 25: (Continued from Figure 24) The third part of the fault-tolerant quantum circuit of stabilizer measurement of $[[7, 1, 3]]$ Steane code: Fault-tolerant preparation of the logical state $|0\rangle_L$. Note that the rectangles, rounded rectangles, hexagons and bi-directed arrow respectively indicate H , $PrepZ$, $MeasZ$ and $SWAP$ gates.

dummy [13]	data [5]	dummy [10]	data [1]	dummy [5]	dummy [18]	dummy [15]
dummy [3]	dummy [2]	syndrome [5]	syndrome [1]	dummy [6]	data [0]	dummy [14]
dummy [11]	data [3]	dummy [16]	dummy [7]	syndrome [0]	dummy [17]	dummy [19]
dummy [0]	syndrome [3]	checkup [0]	dummy [4]	dummy [1]	dummy [9]	data [2]
data [6]	dummy [8]	syndrome [6]	syndrome [4]	syndrome [2]	data [4]	dummy [12]

(a) Step 31

dummy [13]	data [5]	syndrome [5]	data [1]	dummy [5]	dummy [18]	dummy [15]
dummy [3]	dummy [2]	dummy [10]	syndrome [1]	data [0]	dummy [6]	dummy [14]
dummy [11]	data [3]	dummy [16]	dummy [7]	syndrome [0]	dummy [17]	dummy [19]
dummy [0]	syndrome [3]	checkup [0]	dummy [4]	syndrome [2]	dummy [9]	data [2]
data [6]	syndrome [6]	dummy [8]	syndrome [4]	dummy [1]	data [4]	dummy [12]

(b) Step 32

dummy [13]	data [5]	syndrome [5]	dummy [5]	data [1]	dummy [18]	dummy [15]
dummy [3]	data [3]	dummy [10]	syndrome [1]	data [0]	dummy [6]	dummy [14]
dummy [11]	dummy [2]	dummy [16]	dummy [7]	syndrome [0]	dummy [17]	dummy [19]
dummy [0]	syndrome [3]	checkup [0]	dummy [4]	dummy [9]	syndrome [2]	data [2]
data [6]	syndrome [6]	dummy [8]	dummy [1]	syndrome [4]	data [4]	dummy [12]

(c) Step 33

data [5]	dummy [13]	syndrome [5]	dummy [5]	data [1]	dummy [18]	dummy [15]
dummy [3]	data [3]	dummy [10]	syndrome [1]	dummy [6]	data [0]	dummy [14]
dummy [11]	dummy [2]	dummy [16]	dummy [7]	syndrome [0]	dummy [17]	dummy [19]
data [6]	syndrome [3]	checkup [0]	dummy [4]	dummy [9]	syndrome [2]	data [2]
dummy [0]	syndrome [6]	dummy [8]	dummy [1]	syndrome [4]	data [4]	dummy [12]

(d) Step 34

data [5]	data [3]	syndrome [5]	dummy [5]	data [1]	data [0]	dummy [15]
dummy [3]	dummy [13]	dummy [10]	syndrome [1]	dummy [6]	dummy [18]	dummy [14]
dummy [11]	dummy [2]	dummy [16]	dummy [7]	syndrome [0]	dummy [17]	data [2]
data [6]	syndrome [3]	checkup [0]	dummy [4]	dummy [9]	syndrome [2]	dummy [19]
dummy [0]	syndrome [6]	dummy [8]	dummy [1]	syndrome [4]	dummy [12]	data [4]

(e) Step 35

data [5]	data [3]	syndrome [5]	dummy [5]	data [1]	data [0]	dummy [15]
dummy [3]	dummy [13]	dummy [10]	syndrome [1]	dummy [6]	dummy [18]	data [2]
dummy [11]	dummy [2]	dummy [16]	dummy [7]	syndrome [0]	dummy [17]	dummy [14]
data [6]	syndrome [3]	checkup [0]	dummy [4]	dummy [9]	syndrome [2]	dummy [19]
dummy [0]	syndrome [6]	dummy [8]	dummy [1]	syndrome [4]	dummy [12]	data [4]

(f) Final Qubit Mapping

Figure 26: The fourth part of the fault-tolerant quantum circuit of stabilizer measurement of $[[7, 1, 3]]$ Steane code: Transversal *CNOT* between data qubits and syndrome qubits. By the *Move-Back* operations, the data qubits after all the quantum operations are placed in their initial positions (see Figure 16). Note that the rectangles, rounded rectangles, hexagons and bi-directed arrow respectively indicate *H*, *PrepZ*, *MeasZ* and *SWAP* gates.

```

{
  "circuit" : {
    "0" : ["PrepZ 18", "PrepZ 11", "PrepZ 23", "PrepZ 9", "PrepZ 26", "PrepZ 2",
      "PrepZ 16", "PrepZ 17", "SWAP 20,13", "SWAP 6,5", "SWAP 22,21", "SWAP 33,34"],
    "1" : ["H 18", "H 26", "H 2", "H 16", "SWAP 27,20", "SWAP 5,4", "SWAP 32,33"],
    "2" : ["CNOT 18,11", "CNOT 2,9", "CNOT 16,23", "SWAP 19,26"],
    "3" : ["CNOT 16,9", "SWAP 24,23", "SWAP 12,11", "SWAP 25,18"],
    "4" : ["CNOT 19,12", "CNOT 25,24", "SWAP 8,9", "SWAP 23,16"],
    "5" : ["SWAP 18,25", "SWAP 11,12", "SWAP 26,19", "SWAP 31,24", "SWAP 9,2", "SWAP 7,8"],
    "6" : ["CNOT 17,18", "SWAP 25,26", "SWAP 10,11"],
    "7" : ["CNOT 9,10", "SWAP 16,17", "SWAP 24,25"],
    "8" : ["CNOT 16,9", "CNOT 24,23"],
    "9" : ["CNOT 16,23"],
    "10" : ["H 16"],
    "11" : ["MeasZ 16", "Barrier"],
    "12" : ["CNOT 22,23", "SWAP 13,6", "SWAP 8,1", "SWAP 4,5", "SWAP 25,32", "SWAP 34,27", "SWAP 19,18"],
    "13" : ["MeasZ 23", "CNOT 8,7", "SWAP 12,13", "SWAP 1,0", "CNOT 25,24", "SWAP 3,4", "SWAP 32,31"],
    "14" : ["MeasZ 7", "SWAP 2,1", "MeasZ 24", "CNOT 3,10", "CNOT 12,19", "SWAP 33,32"],
    "15" : ["CNOT 2,9", "MeasZ 10", "MeasZ 19", "CNOT 34,33"],
    "16" : ["MeasZ 9", "MeasZ 33", "Barrier"],
    "17" : ["PrepZ 19", "PrepZ 10", "PrepZ 33", "PrepZ 7", "PrepZ 24", "PrepZ 9", "PrepZ 23", "PrepZ 16",
      "SWAP 15,8", "SWAP 27,34", "SWAP 1,2", "SWAP 26,25", "SWAP 21,22"],
    "18" : ["H 10", "H 33", "H 7", "SWAP 18,19", "SWAP 8,9", "SWAP 30,23", "SWAP 28,21"],
    "19" : ["SWAP 17,10", "CNOT 7,8", "SWAP 32,33", "SWAP 31,30"],
    "20" : ["CNOT 17,18", "SWAP 9,8", "CNOT 32,31", "SWAP 14,7", "SWAP 33,26"],
    "21" : ["CNOT 17,24", "SWAP 25,18", "SWAP 30,31", "SWAP 21,14"],
    "22" : ["SWAP 10,17", "CNOT 32,25", "SWAP 23,24", "SWAP 29,30", "SWAP 22,21"],
    "23" : ["CNOT 10,9", "SWAP 18,25", "SWAP 17,16", "CNOT 22,29", "SWAP 30,23"],
    "24" : ["CNOT 18,17", "CNOT 29,30"],
    "25" : ["SWAP 16,17", "SWAP 31,30"],
    "26" : ["CNOT 9,16", "SWAP 30,29"],
    "27" : ["SWAP 23,16"],
    "28" : ["CNOT 30,23"],
    "29" : ["MeasZ 23", "Barrier"],
    "30" : ["CNOT 10,3", "CNOT 22,15", "SWAP 11,12", "SWAP 2,9", "SWAP 25,32", "SWAP 29,30",
      "SWAP 20,13"],
    "31" : ["H 10", "H 22", "CNOT 18,11", "CNOT 2,1", "CNOT 29,28", "SWAP 26,25",
      "SWAP 32,31", "SWAP 4,3", "SWAP 6,13", "SWAP 8,15"],
    "32" : ["MeasZ 10", "MeasZ 22", "H 18", "H 2", "H 29", "CNOT 26,27", "CNOT 32,33",
      "SWAP 12,11", "SWAP 0,1", "SWAP 21,28"],
    "33" : ["MeasZ 18", "MeasZ 2", "H 26", "H 32", "MeasZ 29",
      "SWAP 5,12", "SWAP 34,33", "SWAP 20,27", "SWAP 1,8"],
    "34" : ["MeasZ 26", "MeasZ 32", "SWAP 13,20"],
  },
  "final_mapping" : {"data0" : 5, "data1" : 4, "data2" : 13, "data3" : 1, "data4" : 34,
    "data5" : 0, "data6" : 21},
  "initial_mapping" : {"data0" : 5, "data1" : 4, "data2" : 13, "data3" : 1, "data4" : 34,
    "data5" : 0, "data6" : 21,
    "syndrome0" : 18, "syndrome1" : 11, "syndrome2" : 23, "syndrome3" : 9,
    "syndrome4" : 26, "syndrome5" : 2, "syndrome6" : 16}
}

```

Figure 27: The JSON format representation of the fault-tolerant quantum circuit shown in Figures 20 ~ 26.

LQ1-data[5]	LQ1-data[3]	LQ1-syndrome[5]	LQ1-dummy[5]	LQ1-data[1]	LQ1-data[0]	LQ1-dummy[18]
LQ1-dummy[13]	LQ1-dummy[10]	LQ1-syndrome[3]	LQ1-dummy[6]	LQ1-syndrome[1]	LQ1-dummy[14]	LQ1-data[2]
LQ1-dummy[3]	LQ1-dummy[2]	LQ1-syndrome[6]	LQ1-checkup[0]	LQ1-syndrome[0]	LQ1-dummy[17]	LQ1-dummy[15]
LQ1-data[6]	LQ1-dummy[0]	LQ1-syndrome[2]	LQ1-dummy[7]	LQ1-dummy[1]	LQ1-syndrome[4]	LQ1-dummy[19]
LQ1-dummy[11]	LQ1-dummy[16]	LQ1-dummy[4]	LQ1-dummy[8]	LQ1-dummy[9]	LQ1-dummy[12]	LQ1-data[4]
LQ2-data[5]	LQ2-data[3]	LQ2-syndrome[5]	LQ2-dummy[5]	LQ2-data[1]	LQ2-data[0]	LQ2-dummy[18]
LQ2-dummy[13]	LQ2-dummy[10]	LQ2-syndrome[3]	LQ2-dummy[6]	LQ2-syndrome[1]	LQ2-dummy[14]	LQ2-data[2]
LQ2-dummy[3]	LQ2-dummy[2]	LQ2-syndrome[6]	LQ2-checkup[0]	LQ2-syndrome[0]	LQ2-dummy[17]	LQ2-dummy[15]
LQ2-data[6]	LQ2-dummy[0]	LQ2-syndrome[2]	LQ2-dummy[7]	LQ2-dummy[1]	LQ2-syndrome[4]	LQ2-dummy[19]
LQ2-dummy[11]	LQ2-dummy[16]	LQ2-dummy[4]	LQ2-dummy[8]	LQ2-dummy[9]	LQ2-dummy[12]	LQ2-data[4]

(a) Initial Mapping based on Vertically Extended Layout

LQ1-dummy[13]	LQ1-dummy[10]	LQ1-syndrome[5]	LQ1-dummy[5]	LQ1-syndrome[1]	LQ1-dummy[14]	LQ1-dummy[18]
LQ1-data[5]	LQ1-data[3]	LQ1-syndrome[3]	LQ1-dummy[6]	LQ1-data[1]	LQ1-data[0]	LQ1-dummy[15]
LQ1-dummy[3]	LQ1-dummy[2]	LQ1-syndrome[6]	LQ1-checkup[0]	LQ1-syndrome[0]	LQ1-dummy[17]	LQ1-data[2]
LQ1-data[6]	LQ1-dummy[0]	LQ1-syndrome[2]	LQ1-dummy[7]	LQ1-dummy[1]	LQ1-syndrome[4]	LQ1-dummy[19]
LQ2-data[5]	LQ2-data[3]	LQ1-dummy[4]	LQ1-dummy[8]	LQ2-data[1]	LQ2-data[0]	LQ2-dummy[18]
LQ1-dummy[11]	LQ1-dummy[16]	LQ2-syndrome[5]	LQ2-dummy[5]	LQ1-dummy[9]	LQ1-dummy[12]	LQ1-data[4]
LQ2-dummy[13]	LQ2-dummy[10]	LQ2-syndrome[3]	LQ2-dummy[6]	LQ2-syndrome[1]	LQ2-dummy[14]	LQ2-data[2]
LQ2-data[6]	LQ2-dummy[2]	LQ2-syndrome[6]	LQ2-checkup[0]	LQ2-syndrome[0]	LQ2-dummy[17]	LQ2-dummy[15]
LQ2-dummy[3]	LQ2-dummy[0]	LQ2-syndrome[2]	LQ2-dummy[7]	LQ2-dummy[1]	LQ2-syndrome[4]	LQ2-data[4]
LQ2-dummy[11]	LQ2-dummy[16]	LQ2-dummy[4]	LQ2-dummy[8]	LQ2-dummy[9]	LQ2-dummy[12]	LQ2-dummy[19]

(b) Step 1

LQ1-dummy[13]	LQ1-dummy[10]	LQ1-syndrome[5]	LQ1-dummy[5]	LQ1-syndrome[1]	LQ1-dummy[14]	LQ1-dummy[15]
LQ1-dummy[3]	LQ1-dummy[2]	LQ1-syndrome[3]	LQ1-dummy[6]	LQ1-syndrome[0]	LQ1-dummy[17]	LQ1-dummy[18]
LQ1-data[5]	LQ1-data[3]	LQ1-syndrome[6]	LQ1-checkup[0]	LQ1-data[1]	LQ1-data[0]	LQ1-dummy[19]
LQ1-data[6]	LQ2-data[3]	LQ1-syndrome[2]	LQ1-dummy[7]	LQ2-data[1]	LQ2-data[0]	LQ1-data[2]
LQ2-data[5]	LQ1-dummy[0]	LQ1-dummy[4]	LQ1-dummy[8]	LQ1-dummy[1]	LQ1-syndrome[4]	LQ2-dummy[18]
LQ1-dummy[11]	LQ2-syndrome[5]	LQ1-dummy[16]	LQ2-dummy[5]	LQ1-dummy[9]	LQ1-data[4]	LQ1-dummy[12]
LQ2-data[6]	LQ2-dummy[10]	LQ2-syndrome[3]	LQ2-dummy[6]	LQ2-syndrome[1]	LQ2-dummy[14]	LQ2-data[2]
LQ2-dummy[13]	LQ2-dummy[2]	LQ2-syndrome[6]	LQ2-checkup[0]	LQ2-syndrome[0]	LQ2-dummy[17]	LQ2-data[4]
LQ2-dummy[3]	LQ2-dummy[0]	LQ2-syndrome[2]	LQ2-dummy[7]	LQ2-dummy[1]	LQ2-syndrome[4]	LQ2-dummy[15]
LQ2-dummy[11]	LQ2-dummy[16]	LQ2-dummy[4]	LQ2-dummy[8]	LQ2-dummy[9]	LQ2-dummy[12]	LQ2-dummy[19]

(c) Step 2

LQ1-dummy[3]	LQ1-dummy[10]	LQ1-syndrome[5]	LQ1-dummy[5]	LQ1-syndrome[1]	LQ1-dummy[14]	LQ1-dummy[15]
LQ1-dummy[13]	LQ1-dummy[2]	LQ1-syndrome[3]	LQ1-dummy[6]	LQ1-syndrome[0]	LQ1-dummy[17]	LQ1-dummy[19]
LQ1-data[5]	LQ1-data[3]	LQ1-syndrome[6]	LQ1-checkup[0]	LQ1-data[1]	LQ1-data[0]	LQ1-dummy[18]
LQ1-data[6]	LQ2-data[3]	LQ1-syndrome[2]	LQ1-dummy[7]	LQ2-data[1]	LQ2-data[0]	LQ2-dummy[18]
LQ1-dummy[0]	LQ2-data[5]	LQ1-dummy[4]	LQ1-dummy[8]	LQ1-dummy[1]	LQ1-syndrome[4]	LQ1-data[2]
LQ2-data[6]	LQ2-syndrome[5]	LQ1-dummy[16]	LQ2-dummy[5]	LQ1-dummy[9]	LQ2-dummy[14]	LQ2-data[2]
LQ1-dummy[11]	LQ2-dummy[10]	LQ2-syndrome[3]	LQ2-dummy[6]	LQ2-syndrome[1]	LQ1-data[4]	LQ1-dummy[12]
LQ2-dummy[3]	LQ2-dummy[2]	LQ2-syndrome[6]	LQ2-checkup[0]	LQ2-syndrome[0]	LQ2-dummy[17]	LQ2-data[4]
LQ2-dummy[13]	LQ2-dummy[0]	LQ2-syndrome[2]	LQ2-dummy[7]	LQ2-dummy[1]	LQ2-syndrome[4]	LQ2-dummy[19]
LQ2-dummy[11]	LQ2-dummy[16]	LQ2-dummy[4]	LQ2-dummy[8]	LQ2-dummy[9]	LQ2-dummy[12]	LQ2-dummy[15]

(d) Step 3

Figure 28: Logical *CNOT* gate operations for qubits arranged vertically. (a) The vertically extended qubit layout of logical qubits, LQ1 and LQ2. Note that the bi-directed arrow indicates *SWAP* gate.

LQ1-dummy [3]	LQ1-dummy [10]	LQ1-syndrome [5]	LQ1-dummy [5]	LQ1-syndrome [1]	LQ1-dummy [14]	LQ1-dummy [15]
LQ1-dummy [13]	LQ1-data [3]	LQ1-syndrome [3]	LQ1-dummy [6]	LQ1-data [1]	LQ1-data [0]	LQ1-dummy [19]
LQ1-data [5]	LQ1-dummy [2]	LQ1-syndrome [6]	LQ1-checkup [0]	LQ1-syndrome [0]	LQ1-dummy [17]	LQ1-dummy [18]
LQ1-dummy [0]	LQ2-data [3]	LQ1-syndrome [2]	LQ1-dummy [7]	LQ1-dummy [1]	LQ2-data [0]	LQ2-dummy [18]
LQ1-data [6]	LQ2-data [5]	LQ1-dummy [4]	LQ1-dummy [8]	LQ2-data [1]	LQ2-dummy [14]	LQ1-data [2]
LQ2-data [6]	LQ2-syndrome [5]	LQ1-dummy [16]	LQ2-dummy [5]	LQ1-dummy [9]	LQ1-syndrome [4]	LQ2-data [2]
LQ1-dummy [11]	LQ2-dummy [10]	LQ2-syndrome [3]	LQ2-dummy [6]	LQ2-syndrome [1]	LQ1-data [4]	LQ2-data [4]
LQ2-dummy [3]	LQ2-dummy [2]	LQ2-syndrome [6]	LQ2-checkup [0]	LQ2-syndrome [0]	LQ2-dummy [17]	LQ1-dummy [12]
LQ2-dummy [13]	LQ2-dummy [0]	LQ2-syndrome [2]	LQ2-dummy [7]	LQ2-dummy [1]	LQ2-syndrome [4]	LQ2-dummy [19]
LQ2-dummy [11]	LQ2-dummy [16]	LQ2-dummy [4]	LQ2-dummy [8]	LQ2-dummy [9]	LQ2-dummy [12]	LQ2-dummy [15]

(a) Step 4

LQ1-dummy [3]	LQ1-data [3]	LQ1-syndrome [5]	LQ1-dummy [5]	LQ1-data [1]	LQ1-data [0]	LQ1-dummy [15]
LQ1-dummy [13]	LQ1-dummy [10]	LQ1-syndrome [3]	LQ1-dummy [6]	LQ1-syndrome [1]	LQ1-dummy [14]	LQ1-dummy [19]
LQ1-dummy [0]	LQ2-data [3]	LQ1-syndrome [6]	LQ1-checkup [0]	LQ1-syndrome [0]	LQ1-dummy [17]	LQ1-dummy [18]
LQ1-data [5]	LQ1-dummy [2]	LQ1-syndrome [2]	LQ1-dummy [7]	LQ1-dummy [1]	LQ2-dummy [14]	LQ1-data [2]
LQ1-data [6]	LQ2-data [5]	LQ1-dummy [4]	LQ1-dummy [8]	LQ1-dummy [9]	LQ2-data [0]	LQ2-dummy [18]
LQ2-data [6]	LQ2-syndrome [5]	LQ1-dummy [16]	LQ2-dummy [5]	LQ2-data [1]	LQ1-syndrome [4]	LQ2-data [2]
LQ1-dummy [11]	LQ2-dummy [10]	LQ2-syndrome [3]	LQ2-dummy [6]	LQ2-syndrome [1]	LQ1-data [4]	LQ2-data [4]
LQ2-dummy [3]	LQ2-dummy [2]	LQ2-syndrome [6]	LQ2-checkup [0]	LQ2-syndrome [0]	LQ2-dummy [17]	LQ1-dummy [12]
LQ2-dummy [13]	LQ2-dummy [0]	LQ2-syndrome [2]	LQ2-dummy [7]	LQ2-dummy [1]	LQ2-syndrome [4]	LQ2-dummy [19]
LQ2-dummy [11]	LQ2-dummy [16]	LQ2-dummy [4]	LQ2-dummy [8]	LQ2-dummy [9]	LQ2-dummy [12]	LQ2-dummy [15]

(b) Step 5

LQ1-dummy [3]	LQ1-data [3]	LQ1-syndrome [5]	LQ1-dummy [5]	LQ1-data [1]	LQ1-data [0]	LQ1-dummy [15]
LQ1-dummy [13]	LQ1-dummy [10]	LQ1-syndrome [3]	LQ1-dummy [6]	LQ1-syndrome [1]	LQ1-dummy [14]	LQ1-dummy [19]
LQ1-dummy [0]	LQ2-data [3]	LQ1-syndrome [6]	LQ1-checkup [0]	LQ1-syndrome [0]	LQ1-dummy [17]	LQ1-data [2]
LQ1-data [5]	LQ2-data [5]	LQ1-syndrome [2]	LQ1-dummy [7]	LQ1-dummy [1]	LQ2-dummy [14]	LQ1-dummy [18]
LQ1-data [6]	LQ1-dummy [2]	LQ1-dummy [4]	LQ1-dummy [8]	LQ1-dummy [9]	LQ1-syndrome [4]	LQ2-dummy [18]
LQ1-dummy [11]	LQ2-syndrome [5]	LQ1-dummy [16]	LQ2-dummy [5]	LQ2-data [1]	LQ2-data [0]	LQ2-data [2]
LQ2-data [6]	LQ2-dummy [10]	LQ2-syndrome [3]	LQ2-dummy [6]	LQ2-syndrome [1]	LQ1-data [4]	LQ1-dummy [12]
LQ2-dummy [3]	LQ2-dummy [2]	LQ2-syndrome [6]	LQ2-checkup [0]	LQ2-syndrome [0]	LQ2-dummy [17]	LQ2-data [4]
LQ2-dummy [13]	LQ2-dummy [0]	LQ2-syndrome [2]	LQ2-dummy [7]	LQ2-dummy [1]	LQ2-syndrome [4]	LQ2-dummy [19]
LQ2-dummy [11]	LQ2-dummy [16]	LQ2-dummy [4]	LQ2-dummy [8]	LQ2-dummy [9]	LQ2-dummy [12]	LQ2-dummy [15]

(c) Step 6

LQ1-dummy [3]	LQ1-data [3]	LQ1-syndrome [5]	LQ1-dummy [5]	LQ1-data [1]	LQ1-data [0]	LQ1-dummy [15]
LQ1-dummy [13]	LQ1-dummy [10]	LQ1-syndrome [3]	LQ1-dummy [6]	LQ1-syndrome [1]	LQ1-dummy [14]	LQ1-data [2]
LQ1-dummy [0]	LQ2-data [3]	LQ1-syndrome [6]	LQ1-checkup [0]	LQ1-syndrome [0]	LQ1-dummy [17]	LQ1-dummy [19]
LQ1-data [5]	LQ2-data [5]	LQ1-syndrome [2]	LQ1-dummy [7]	LQ1-dummy [1]	LQ2-dummy [14]	LQ1-dummy [18]
LQ1-data [6]	LQ2-syndrome [5]	LQ1-dummy [4]	LQ1-dummy [8]	LQ1-dummy [9]	LQ1-syndrome [4]	LQ2-dummy [18]
LQ1-dummy [11]	LQ1-dummy [2]	LQ1-dummy [16]	LQ2-dummy [5]	LQ2-data [1]	LQ2-data [0]	LQ1-dummy [12]
LQ2-dummy [3]	LQ2-dummy [10]	LQ2-syndrome [3]	LQ2-dummy [6]	LQ2-syndrome [1]	LQ1-data [4]	LQ2-data [2]
LQ2-data [6]	LQ2-dummy [2]	LQ2-syndrome [6]	LQ2-checkup [0]	LQ2-syndrome [0]	LQ2-dummy [17]	LQ2-dummy [19]
LQ2-dummy [13]	LQ2-dummy [0]	LQ2-syndrome [2]	LQ2-dummy [7]	LQ2-dummy [1]	LQ2-syndrome [4]	LQ2-data [4]
LQ2-dummy [11]	LQ2-dummy [16]	LQ2-dummy [4]	LQ2-dummy [8]	LQ2-dummy [9]	LQ2-dummy [12]	LQ2-dummy [15]

(d) Step 7

Figure 29: (Continued from Figure 28) Logical *CNOT* gate operations for qubits arranged vertically. Note that the bi-directed arrow indicates *SWAP* gate.

LQ1-dummy [3]	LQ1-data [3]	LQ1-syndrome [5]	LQ1-dummy [5]	LQ1-data [1]	LQ1-data [0]	LQ1-dummy [15]
LQ1-dummy [13]	LQ1-dummy [10]	LQ1-syndrome [3]	LQ1-dummy [6]	LQ1-syndrome [1]	LQ1-dummy [14]	LQ1-data [2]
LQ1-data [5]	LQ2-data [3]	LQ1-syndrome [6]	LQ1-checkup [0]	LQ1-syndrome [0]	LQ1-dummy [17]	LQ1-dummy [19]
LQ1-dummy [0]	LQ2-syndrome [5]	LQ1-syndrome [2]	LQ1-dummy [7]	LQ1-dummy [1]	LQ2-dummy [14]	LQ1-dummy [18]
LQ1-data [6]	LQ2-data [5]	LQ1-dummy [4]	LQ1-dummy [8]	LQ1-dummy [9]	LQ1-syndrome [4]	LQ1-dummy [12]
LQ1-dummy [11]	LQ2-dummy [10]	LQ1-dummy [16]	LQ2-dummy [5]	LQ2-data [1]	LQ2-data [0]	LQ2-dummy [18]
LQ2-dummy [3]	LQ1-dummy [2]	LQ2-syndrome [3]	LQ2-dummy [6]	LQ2-syndrome [1]	LQ1-data [4]	LQ2-data [2]
LQ2-dummy [13]	LQ2-dummy [2]	LQ2-syndrome [6]	LQ2-checkup [0]	LQ2-syndrome [0]	LQ2-dummy [17]	LQ2-dummy [19]
LQ2-data [6]	LQ2-dummy [0]	LQ2-syndrome [2]	LQ2-dummy [7]	LQ2-dummy [1]	LQ2-syndrome [4]	LQ2-dummy [15]
LQ2-dummy [11]	LQ2-dummy [16]	LQ2-dummy [4]	LQ2-dummy [8]	LQ2-dummy [9]	LQ2-dummy [12]	LQ2-data [4]

(a) Step 8

LQ1-dummy [3]	LQ1-data [3]	LQ1-syndrome [5]	LQ1-dummy [5]	LQ1-data [1]	LQ1-data [0]	LQ1-dummy [15]
LQ1-data [5]	LQ1-dummy [10]	LQ1-syndrome [3]	LQ1-dummy [6]	LQ1-syndrome [1]	LQ1-dummy [14]	LQ1-data [2]
LQ1-dummy [13]	LQ2-syndrome [5]	LQ1-syndrome [6]	LQ1-checkup [0]	LQ1-syndrome [0]	LQ1-dummy [17]	LQ1-dummy [19]
LQ1-data [6]	LQ2-data [3]	LQ1-syndrome [2]	LQ1-dummy [7]	LQ1-dummy [1]	LQ2-dummy [14]	LQ1-dummy [18]
LQ1-dummy [0]	LQ2-data [5]	LQ1-dummy [4]	LQ1-dummy [8]	LQ1-dummy [9]	LQ1-dummy [12]	LQ1-syndrome [4]
LQ2-dummy [10]	LQ1-dummy [11]	LQ1-dummy [16]	LQ2-dummy [5]	LQ2-data [1]	LQ2-data [0]	LQ2-dummy [18]
LQ2-dummy [3]	LQ1-dummy [2]	LQ2-syndrome [3]	LQ2-dummy [6]	LQ2-syndrome [1]	LQ1-data [4]	LQ2-data [2]
LQ2-dummy [13]	LQ2-dummy [2]	LQ2-syndrome [6]	LQ2-checkup [0]	LQ2-syndrome [0]	LQ2-dummy [17]	LQ2-dummy [19]
LQ2-data [6]	LQ2-dummy [0]	LQ2-syndrome [2]	LQ2-dummy [7]	LQ2-dummy [1]	LQ2-syndrome [4]	LQ2-dummy [15]
LQ2-dummy [11]	LQ2-dummy [16]	LQ2-dummy [4]	LQ2-dummy [8]	LQ2-dummy [9]	LQ2-dummy [12]	LQ2-data [4]

(b) Step 9

LQ1-data [5]	LQ1-data [3]	LQ1-syndrome [5]	LQ1-dummy [5]	LQ1-data [1]	LQ1-data [0]	LQ1-dummy [15]
LQ1-dummy [3]	LQ1-dummy [10]	LQ1-syndrome [3]	LQ1-dummy [6]	LQ1-syndrome [1]	LQ1-dummy [14]	LQ1-data [2]
LQ1-dummy [13]	LQ2-syndrome [5]	LQ1-syndrome [6]	LQ1-checkup [0]	LQ1-syndrome [0]	LQ1-dummy [17]	LQ1-dummy [19]
LQ1-data [6]	LQ2-data [3]	LQ1-syndrome [2]	LQ1-dummy [7]	LQ1-dummy [1]	LQ2-dummy [14]	LQ1-dummy [18]
LQ1-dummy [0]	LQ1-dummy [11]	LQ1-dummy [4]	LQ1-dummy [8]	LQ1-dummy [9]	LQ2-data [0]	LQ1-syndrome [4]
LQ2-dummy [10]	LQ2-data [5]	LQ1-dummy [16]	LQ2-dummy [5]	LQ2-data [1]	LQ1-dummy [12]	LQ2-dummy [18]
LQ2-dummy [3]	LQ1-dummy [2]	LQ2-syndrome [3]	LQ2-dummy [6]	LQ2-syndrome [1]	LQ1-data [4]	LQ2-data [2]
LQ2-dummy [13]	LQ2-dummy [2]	LQ2-syndrome [6]	LQ2-checkup [0]	LQ2-syndrome [0]	LQ2-dummy [17]	LQ2-dummy [19]
LQ2-data [6]	LQ2-dummy [0]	LQ2-syndrome [2]	LQ2-dummy [7]	LQ2-dummy [1]	LQ2-syndrome [4]	LQ2-dummy [15]
LQ2-dummy [11]	LQ2-dummy [16]	LQ2-dummy [4]	LQ2-dummy [8]	LQ2-dummy [9]	LQ2-dummy [12]	LQ2-data [4]

(c) Step 10

LQ1-data [5]	LQ1-data [3]	LQ1-syndrome [5]	LQ1-dummy [5]	LQ1-data [1]	LQ1-data [0]	LQ1-dummy [15]
LQ1-dummy [3]	LQ1-dummy [10]	LQ1-syndrome [3]	LQ1-dummy [6]	LQ1-syndrome [1]	LQ1-dummy [14]	LQ1-data [2]
LQ1-dummy [13]	LQ2-syndrome [5]	LQ1-syndrome [6]	LQ1-checkup [0]	LQ1-syndrome [0]	LQ1-dummy [17]	LQ1-dummy [19]
LQ1-data [6]	LQ1-dummy [11]	LQ1-syndrome [2]	LQ1-dummy [7]	LQ1-dummy [1]	LQ2-dummy [14]	LQ1-dummy [18]
LQ1-dummy [0]	LQ2-data [3]	LQ1-dummy [4]	LQ1-dummy [8]	LQ1-dummy [9]	LQ2-data [0]	LQ1-syndrome [4]
LQ2-data [5]	LQ2-dummy [10]	LQ1-dummy [16]	LQ2-dummy [5]	LQ2-data [1]	LQ1-data [4]	LQ2-dummy [18]
LQ2-dummy [3]	LQ1-dummy [2]	LQ2-syndrome [3]	LQ2-dummy [6]	LQ2-syndrome [1]	LQ1-dummy [12]	LQ2-data [2]
LQ2-dummy [13]	LQ2-dummy [2]	LQ2-syndrome [6]	LQ2-checkup [0]	LQ2-syndrome [0]	LQ2-dummy [17]	LQ2-dummy [19]
LQ2-data [6]	LQ2-dummy [0]	LQ2-syndrome [2]	LQ2-dummy [7]	LQ2-dummy [1]	LQ2-syndrome [4]	LQ2-dummy [15]
LQ2-dummy [11]	LQ2-dummy [16]	LQ2-dummy [4]	LQ2-dummy [8]	LQ2-dummy [9]	LQ2-dummy [12]	LQ2-data [4]

(d) Step 11

Figure 30: (Continued from Figure 29) Logical *CNOT* gate operations for qubits arranged vertically. Note that the bi-directed arrow indicates *SWAP* gate.

LQ1-data[5]	LQ1-data[3]	LQ1-syndrome[5]	LQ1-dummy[5]	LQ1-data[1]	LQ1-data[0]	LQ1-dummy[15]
LQ1-dummy[3]	LQ1-dummy[10]	LQ1-syndrome[3]	LQ1-dummy[6]	LQ1-syndrome[1]	LQ1-dummy[14]	LQ1-data[2]
LQ1-dummy[13]	LQ2-syndrome[5]	LQ1-syndrome[6]	LQ1-checkup[0]	LQ1-syndrome[0]	LQ1-dummy[17]	LQ1-dummy[19]
LQ1-data[6]	LQ1-dummy[11]	LQ1-syndrome[2]	LQ1-dummy[7]	LQ1-dummy[1]	LQ2-dummy[14]	LQ1-dummy[18]
LQ1-dummy[0]	LQ2-dummy[10]	LQ1-dummy[4]	LQ1-dummy[8]	LQ1-dummy[9]	LQ2-data[0]	LQ1-syndrome[4]
LQ2-data[5]	LQ2-data[3]	LQ1-dummy[16]	LQ2-dummy[5]	LQ2-data[1]	LQ2-dummy[18]	LQ1-data[4]
LQ2-dummy[3]	LQ1-dummy[2]	LQ2-syndrome[3]	LQ2-dummy[6]	LQ2-syndrome[1]	LQ1-dummy[12]	LQ2-data[2]
LQ2-dummy[13]	LQ2-dummy[2]	LQ2-syndrome[6]	LQ2-checkup[0]	LQ2-syndrome[0]	LQ2-dummy[17]	LQ2-dummy[19]
LQ2-data[6]	LQ2-dummy[0]	LQ2-syndrome[2]	LQ2-dummy[7]	LQ2-dummy[1]	LQ2-syndrome[4]	LQ2-dummy[15]
LQ2-dummy[11]	LQ2-dummy[16]	LQ2-dummy[14]	LQ2-dummy[8]	LQ2-dummy[9]	LQ2-dummy[12]	LQ2-data[4]

(a) Step 12

LQ1-data[5]	LQ1-data[3]	LQ1-syndrome[5]	LQ1-dummy[5]	LQ1-data[1]	LQ1-data[0]	LQ1-dummy[15]
LQ1-dummy[3]	LQ1-dummy[10]	LQ1-syndrome[3]	LQ1-dummy[6]	LQ1-syndrome[1]	LQ1-dummy[14]	LQ1-data[2]
LQ1-dummy[13]	LQ2-syndrome[5]	LQ1-syndrome[6]	LQ1-checkup[0]	LQ1-syndrome[0]	LQ1-dummy[17]	LQ1-dummy[19]
LQ1-data[6]	LQ1-dummy[11]	LQ1-syndrome[2]	LQ1-dummy[7]	LQ1-dummy[1]	LQ2-dummy[14]	LQ1-dummy[18]
LQ1-dummy[0]	LQ2-dummy[10]	LQ1-dummy[4]	LQ1-dummy[8]	LQ1-dummy[9]	LQ2-dummy[18]	LQ1-data[4]
LQ2-data[5]	LQ2-data[3]	LQ1-dummy[16]	LQ2-dummy[5]	LQ2-data[1]	LQ2-data[0]	LQ1-syndrome[4]
LQ2-dummy[3]	LQ1-dummy[2]	LQ2-syndrome[3]	LQ2-dummy[6]	LQ2-syndrome[1]	LQ1-dummy[12]	LQ2-data[2]
LQ2-dummy[13]	LQ2-dummy[2]	LQ2-syndrome[6]	LQ2-checkup[0]	LQ2-syndrome[0]	LQ2-dummy[17]	LQ2-dummy[19]
LQ2-data[6]	LQ2-dummy[0]	LQ2-syndrome[2]	LQ2-dummy[7]	LQ2-dummy[1]	LQ2-syndrome[4]	LQ2-dummy[15]
LQ2-dummy[11]	LQ2-dummy[16]	LQ2-dummy[14]	LQ2-dummy[8]	LQ2-dummy[9]	LQ2-dummy[12]	LQ2-data[4]

(b) Step 13 (Final Qubit Mapping)

Figure 31: (Continued from Figure 30) Logical *CNOT* gate operations for qubits arranged vertically. By the *Move-Back* operations, the data qubits after all the quantum operations are placed in their initial positions (compare (b) and Figure 28 (a)). Note that the bi-directed arrow indicates *SWAP* gate.

LQ1-data[5]	LQ1-data[3]	dummy [16]	dummy [50]	LQ1-data[1]	LQ1-data[0]	dummy [39]
dummy [22]	dummy [37]	dummy [21]	dummy [45]	dummy [11]	dummy [35]	LQ1-data[2]
dummy [10]	dummy [25]	dummy [43]	dummy [49]	dummy [19]	dummy [28]	dummy [32]
LQ1-data[6]	dummy [51]	dummy [33]	dummy [18]	dummy [41]	dummy [53]	dummy [26]
dummy [0]	dummy [42]	dummy [29]	dummy [15]	dummy [38]	dummy [34]	LQ1-data[4]
dummy [31]	LQ2-magic[4]	dummy [9]	dummy [14]	dummy [5]	dummy [47]	dummy [13]
LQ2-magic[3]	dummy [20]	dummy [24]	dummy [55]	LQ2-magic[6]	dummy [46]	LQ2-magic[2]
dummy [30]	LQ2-magic[1]	dummy [40]	dummy [17]	dummy [52]	dummy [1]	dummy [48]
dummy [3]	dummy [36]	dummy [2]	dummy [6]	dummy [8]	dummy [27]	LQ2-magic[0]
dummy [4]	dummy [23]	LQ2-magic[5]	dummy [7]	dummy [54]	dummy [12]	dummy [44]

(a) Initial Mapping based on Vertically Extended Layout, ($data_n, magic_s$)

LQ1-data[5]	LQ1-data[3]	dummy [16]	dummy [50]	LQ1-data[1]	LQ1-data[0]	dummy [39]
dummy [22]	dummy [37]	dummy [21]	dummy [45]	dummy [11]	dummy [35]	LQ1-data[2]
dummy [10]	dummy [25]	dummy [43]	dummy [49]	dummy [19]	dummy [28]	dummy [32]
LQ1-data[6]	dummy [51]	dummy [33]	dummy [18]	dummy [41]	dummy [53]	dummy [26]
dummy [0]	dummy [42]	dummy [29]	dummy [15]	dummy [38]	dummy [34]	LQ1-data[4]
dummy [31]	LQ2-magic[4]	dummy [9]	dummy [14]	dummy [5]	dummy [47]	dummy [13]
LQ2-magic[3]	dummy [20]	dummy [24]	dummy [55]	LQ2-magic[6]	dummy [46]	LQ2-magic[2]
dummy [30]	LQ2-magic[1]	dummy [40]	dummy [17]	dummy [52]	dummy [1]	dummy [48]
dummy [3]	dummy [36]	dummy [2]	dummy [6]	dummy [8]	dummy [27]	LQ2-magic[0]
dummy [4]	dummy [23]	LQ2-magic[5]	dummy [7]	dummy [54]	dummy [12]	dummy [44]

(b) Step 1

dummy [22]	dummy [37]	dummy [16]	dummy [50]	dummy [11]	dummy [35]	dummy [39]
LQ1-data[5]	LQ1-data[3]	dummy [21]	dummy [45]	LQ1-data[1]	LQ1-data[0]	dummy [32]
dummy [10]	dummy [25]	dummy [43]	dummy [49]	dummy [19]	dummy [28]	LQ1-data[2]
LQ1-data[6]	dummy [51]	dummy [33]	dummy [18]	dummy [41]	dummy [53]	dummy [26]
dummy [0]	LQ2-magic[4]	dummy [29]	dummy [15]	dummy [38]	LQ1-data[4]	dummy [34]
dummy [31]	LQ2-magic[1]	dummy [24]	dummy [55]	dummy [5]	dummy [46]	dummy [13]
LQ2-magic[3]	dummy [42]	dummy [9]	dummy [14]	LQ2-magic[6]	dummy [47]	LQ2-magic[2]
dummy [30]	dummy [20]	dummy [40]	dummy [17]	dummy [52]	dummy [1]	LQ2-magic[0]
dummy [3]	dummy [36]	LQ2-magic[5]	dummy [6]	dummy [8]	dummy [27]	dummy [48]
dummy [4]	dummy [23]	dummy [2]	dummy [7]	dummy [54]	dummy [12]	dummy [44]

(c) Step 2

Figure 32: The first part of logical T gate operations for qubits arranged vertically: Trasversal $CNOT$ between data qubits $data[i]$ and magic qubits $magic[i]$ and $MeasZ$ on magic qubits. (a) The vertically extended qubit layout of logical qubits: data qubits in the north direction and magic qubits in the south direction. Note that the rectangles, hexagons and bi-directed arrow respectively indicate S , $PrepZ$, $MeasZ$ and $SWAP$ gates.

dummy [22]	dummy [37]	dummy [16]	dummy [50]	dummy [11]	dummy [35]	dummy [39]
dummy [10]	dummy [25]	dummy [21]	dummy [45]	dummy [19]	dummy [28]	dummy [32]
LQ1-data [5]	LQ1-data [3]	dummy [43]	dummy [49]	LQ1-data [1]	LQ1-data [0]	dummy [26]
LQ1-data [6]	dummy [51]	dummy [33]	dummy [18]	dummy [41]	dummy [53]	LQ1-data [2]
LQ2-magic [3]	dummy [29]	LQ2-magic [4]	dummy [15]	LQ2-magic [6]	LQ1-data [4]	LQ2-magic [2]
dummy [0]	LQ2-magic [1]	dummy [9]	dummy [14]	dummy [38]	dummy [47]	dummy [34]
dummy [31]	dummy [42]	dummy [24]	dummy [55]	dummy [5]	dummy [46]	LQ2-magic [0]
dummy [30]	dummy [20]	LQ2-magic [5]	dummy [17]	dummy [52]	dummy [1]	dummy [13]
dummy [3]	dummy [36]	dummy [40]	dummy [6]	dummy [8]	dummy [27]	dummy [48]
dummy [4]	dummy [23]	dummy [2]	dummy [7]	dummy [54]	dummy [12]	dummy [44]

(a) Step 3

dummy [22]	dummy [37]	dummy [16]	dummy [50]	dummy [11]	dummy [35]	dummy [39]
dummy [10]	dummy [25]	dummy [21]	dummy [45]	dummy [19]	dummy [28]	dummy [32]
LQ1-data [5]	dummy [51]	dummy [43]	dummy [49]	LQ1-data [1]	dummy [53]	dummy [26]
LQ1-data [6]	LQ1-data [3]	dummy [33]	dummy [18]	LQ2-magic [6]	LQ1-data [0]	LQ1-data [2]
LQ2-magic [3]	LQ2-magic [1]	dummy [15]	LQ2-magic [4]	dummy [41]	LQ1-data [4]	LQ2-magic [2]
dummy [0]	dummy [29]	dummy [9]	dummy [14]	dummy [38]	dummy [47]	LQ2-magic [0]
dummy [31]	dummy [42]	LQ2-magic [5]	dummy [55]	dummy [5]	dummy [46]	dummy [34]
dummy [30]	dummy [20]	dummy [24]	dummy [17]	dummy [52]	dummy [1]	dummy [13]
dummy [3]	dummy [36]	dummy [40]	dummy [6]	dummy [8]	dummy [27]	dummy [48]
dummy [4]	dummy [23]	dummy [2]	dummy [7]	dummy [54]	dummy [12]	dummy [44]

(b) Step 4

dummy [22]	dummy [37]	dummy [16]	dummy [50]	dummy [11]	dummy [35]	dummy [39]
dummy [10]	dummy [25]	dummy [21]	dummy [45]	dummy [19]	dummy [28]	dummy [32]
dummy [51]	LQ1-data [5]	dummy [43]	dummy [49]	LQ1-data [1]	dummy [53]	LQ1-data [2]
LQ1-data [6]	LQ1-data [3]	dummy [33]	LQ2-magic [6]	dummy [18]	LQ1-data [0]	dummy [26]
LQ2-magic [3]	dummy [15]	LQ2-magic [1]	dummy [41]	LQ2-magic [4]	LQ1-data [4]	LQ2-magic [2]
dummy [0]	dummy [29]	LQ2-magic [5]	dummy [14]	dummy [38]	dummy [47]	LQ2-magic [0]
dummy [31]	dummy [42]	dummy [9]	dummy [55]	dummy [5]	dummy [46]	dummy [34]
dummy [30]	dummy [20]	dummy [24]	dummy [17]	dummy [52]	dummy [1]	dummy [13]
dummy [3]	dummy [36]	dummy [40]	dummy [6]	dummy [8]	dummy [27]	dummy [48]
dummy [4]	dummy [23]	dummy [2]	dummy [7]	dummy [54]	dummy [12]	dummy [44]

(c) Step 5

Figure 33: (Continued from Figure 32) The first part of logical T gate operations for qubits arranged vertically: Transversal $CNOT$ between data qubits $data[i]$ and magic qubits $magic[i]$ and $MeasZ$ on magic qubits. Note that the rectangles, hexagons and bi-directed arrow respectively indicate S , $PrepZ$, $MeasZ$ and $SWAP$ gates.

dummy [22]	dummy [37]	dummy [16]	dummy [50]	dummy [11]	dummy [35]	dummy [39]
dummy [10]	dummy [25]	dummy [21]	dummy [45]	dummy [19]	dummy [28]	dummy [32]
dummy [51]	dummy [43]	LQ1-data [5]	dummy [49]	dummy [18]	dummy [53]	LQ1-data [2]
LQ1-data [6]	← dummy [15]	LQ2-magic [6]	dummy [33]	LQ1-data [1]	dummy [26]	LQ1-data [0]
LQ2-magic [3]	⊕ LQ1-data [3]	dummy [41]	LQ2-magic [1]	LQ2-magic [4]	LQ1-data [4]	LQ2-magic [0]
dummy [0]	dummy [29]	LQ2-magic [5]	dummy [14]	dummy [38]	dummy [47]	LQ2-magic [2]
dummy [31]	dummy [42]	dummy [9]	dummy [55]	dummy [5]	dummy [46]	dummy [34]
dummy [30]	dummy [20]	dummy [24]	dummy [17]	dummy [52]	dummy [1]	dummy [13]
dummy [3]	dummy [36]	dummy [40]	dummy [6]	dummy [8]	dummy [27]	dummy [48]
dummy [4]	dummy [23]	dummy [2]	dummy [7]	dummy [54]	dummy [12]	dummy [44]

(a) Step 6

dummy [22]	dummy [37]	dummy [16]	dummy [50]	dummy [11]	dummy [35]	dummy [39]
dummy [10]	dummy [25]	dummy [21]	dummy [45]	dummy [19]	dummy [28]	dummy [32]
dummy [51]	dummy [43]	LQ1-data [5]	dummy [49]	dummy [18]	dummy [53]	LQ1-data [2]
dummy [15]	LQ1-data [6]	⊕ LQ2-magic [6]	LQ2-magic [1]	⊕ LQ1-data [1]	dummy [26]	LQ1-data [0]
LQ2-magic [3]	LQ1-data [3]	LQ2-magic [5]	dummy [33]	LQ2-magic [4]	LQ1-data [4]	LQ2-magic [0]
dummy [0]	dummy [29]	dummy [41]	dummy [14]	dummy [38]	dummy [47]	LQ2-magic [2]
dummy [31]	dummy [42]	dummy [9]	dummy [55]	dummy [5]	dummy [46]	dummy [34]
dummy [30]	dummy [20]	dummy [24]	dummy [17]	dummy [52]	dummy [1]	dummy [13]
dummy [3]	dummy [36]	dummy [40]	dummy [6]	dummy [8]	dummy [27]	dummy [48]
dummy [4]	dummy [23]	dummy [2]	dummy [7]	dummy [54]	dummy [12]	dummy [44]

(b) Step 7

dummy [22]	dummy [37]	dummy [16]	dummy [50]	dummy [11]	dummy [35]	dummy [39]
dummy [10]	dummy [25]	dummy [21]	dummy [45]	dummy [19]	dummy [28]	dummy [32]
dummy [51]	dummy [43]	LQ1-data [5]	dummy [49]	dummy [18]	dummy [53]	LQ1-data [2]
dummy [15]	LQ1-data [6]	LQ2-magic [6]	LQ2-magic [1]	LQ1-data [1]	dummy [26]	LQ1-data [0]
LQ2-magic [3]	LQ1-data [3]	LQ2-magic [5]	dummy [33]	LQ2-magic [4]	LQ1-data [4]	LQ2-magic [0]
dummy [0]	dummy [29]	dummy [41]	dummy [14]	dummy [38]	dummy [47]	LQ2-magic [2]
dummy [31]	dummy [42]	dummy [9]	dummy [55]	dummy [5]	dummy [46]	dummy [34]
dummy [30]	dummy [20]	dummy [24]	dummy [17]	dummy [52]	dummy [1]	dummy [13]
dummy [3]	dummy [36]	dummy [40]	dummy [6]	dummy [8]	dummy [27]	dummy [48]
dummy [4]	dummy [23]	dummy [2]	dummy [7]	dummy [54]	dummy [12]	dummy [44]

(c) Step 8

Figure 34: (Continued from Figure 33) The first part of logical T gate operations for qubits arranged vertically: Transversal $CNOT$ between data qubits $data[i]$ and magic qubits $magic[i]$ and $MeasZ$ on magic qubits. Note that the rectangles, hexagons and bi-directed arrow respectively indicate S , $PrepZ$, $MeasZ$ and $SWAP$ gates.

dummy [22]	dummy [37]	dummy [16]	dummy [50]	dummy [11]	dummy [35]	dummy [39]
dummy [10]	dummy [25]	dummy [21]	dummy [45]	dummy [19]	dummy [28]	dummy [32]
dummy [51]	dummy [43]	LQ1-data [5]	dummy [49]	dummy [18]	dummy [53]	LQ1-data [2]
dummy [15]	LQ1-data [6]	LQ2-magic [6]	LQ2-magic [1]	LQ1-data [1]	dummy [26]	LQ1-data [0]
LQ2-magic [3]	LQ1-data [3]	LQ2-magic [5]	dummy [33]	LQ2-magic [4]	LQ1-data [4]	LQ2-magic [0]
dummy [0]	dummy [29]	dummy [41]	dummy [14]	dummy [38]	dummy [47]	LQ2-magic [2]
dummy [31]	dummy [42]	dummy [9]	dummy [55]	dummy [5]	dummy [46]	dummy [34]
dummy [30]	dummy [20]	dummy [24]	dummy [17]	dummy [52]	dummy [1]	dummy [13]
dummy [3]	dummy [36]	dummy [40]	dummy [6]	dummy [8]	dummy [27]	dummy [48]
dummy [4]	dummy [23]	dummy [2]	dummy [7]	dummy [54]	dummy [12]	dummy [44]

(a) Step 9

dummy [22]	dummy [37]	dummy [16]	dummy [50]	dummy [11]	dummy [35]	dummy [39]
dummy [10]	dummy [25]	dummy [21]	dummy [45]	dummy [19]	dummy [28]	dummy [32]
dummy [51]	dummy [43]	LQ1-data [5]	dummy [49]	dummy [18]	dummy [53]	LQ1-data [2]
dummy [15]	LQ1-data [6]	LQ2-magic [5]	LQ2-magic [1]	LQ1-data [1]	dummy [26]	LQ1-data [0]
LQ2-magic [3]	LQ1-data [3]	LQ2-magic [6]	dummy [33]	LQ2-magic [4]	LQ1-data [4]	LQ2-magic [0]
dummy [0]	dummy [29]	dummy [41]	dummy [14]	dummy [38]	dummy [47]	LQ2-magic [2]
dummy [31]	dummy [42]	dummy [9]	dummy [55]	dummy [5]	dummy [46]	dummy [34]
dummy [30]	dummy [20]	dummy [24]	dummy [17]	dummy [52]	dummy [1]	dummy [13]
dummy [3]	dummy [36]	dummy [40]	dummy [6]	dummy [8]	dummy [27]	dummy [48]
dummy [4]	dummy [23]	dummy [2]	dummy [7]	dummy [54]	dummy [12]	dummy [44]

(b) Step 10

dummy [22]	dummy [37]	dummy [16]	dummy [50]	dummy [11]	dummy [35]	dummy [39]
dummy [10]	dummy [25]	dummy [21]	dummy [45]	dummy [19]	dummy [28]	dummy [32]
dummy [51]	dummy [43]	LQ1-data [5]	dummy [49]	dummy [18]	dummy [53]	LQ1-data [2]
dummy [15]	LQ1-data [6]	LQ2-magic [5]	LQ2-magic [1]	LQ1-data [1]	dummy [26]	LQ1-data [0]
LQ2-magic [3]	LQ1-data [3]	LQ2-magic [6]	dummy [33]	LQ2-magic [4]	LQ1-data [4]	LQ2-magic [0]
dummy [0]	dummy [29]	dummy [41]	dummy [14]	dummy [38]	dummy [47]	LQ2-magic [2]
dummy [31]	dummy [42]	dummy [9]	dummy [55]	dummy [5]	dummy [46]	dummy [34]
dummy [30]	dummy [20]	dummy [24]	dummy [17]	dummy [52]	dummy [1]	dummy [13]
dummy [3]	dummy [36]	dummy [40]	dummy [6]	dummy [8]	dummy [27]	dummy [48]
dummy [4]	dummy [23]	dummy [2]	dummy [7]	dummy [54]	dummy [12]	dummy [44]

(c) Step 11 (Barrier)

Figure 35: (Continued from Figure 34) The first part of logical T gate operations for qubits arranged vertically: Transversal $CNOT$ between data qubits $data[i]$ and magic qubits $magic[i]$ and $MeasZ$ on magic qubits. Note that the rectangles, hexagons and bi-directed arrow respectively indicate S , $PrepZ$, $MeasZ$ and $SWAP$ gates.

dummy [22]	dummy [37]	dummy [16]	dummy [50]	dummy [11]	dummy [35]	dummy [39]
dummy [10]	dummy [25]	dummy [21]	dummy [45]	dummy [19]	dummy [28]	dummy [32]
dummy [51]	dummy [43]	LQ1-data [5]	dummy [49]	dummy [18]	dummy [53]	LQ1-data [2]
dummy [15]	LQ1-data [6]	LQ2-magic [5]	LQ2-magic [1]	LQ1-data [1]	dummy [26]	LQ1-data [0]
LQ2-magic [3]	LQ1-data [3]	LQ2-magic [6]	dummy [33]	LQ2-magic [4]	LQ1-data [4]	LQ2-magic [0]
dummy [0]	dummy [29]	dummy [41]	dummy [14]	dummy [38]	dummy [47]	LQ2-magic [2]
dummy [31]	dummy [42]	dummy [9]	dummy [55]	dummy [5]	dummy [46]	dummy [34]
dummy [30]	dummy [20]	dummy [24]	dummy [17]	dummy [52]	dummy [1]	dummy [13]
dummy [3]	dummy [36]	dummy [40]	dummy [6]	dummy [8]	dummy [27]	dummy [48]
dummy [4]	dummy [23]	dummy [2]	dummy [7]	dummy [54]	dummy [12]	dummy [44]

(a) Step 12 (S-correction)

dummy [22]	dummy [37]	dummy [16]	dummy [50]	dummy [11]	dummy [35]	dummy [39]
dummy [10]	dummy [25]	dummy [21]	dummy [45]	dummy [19]	dummy [28]	dummy [32]
dummy [51]	dummy [43]	LQ1-data [5]	dummy [49]	dummy [18]	dummy [53]	LQ1-data [2]
dummy [15]	LQ1-data [6]	LQ2-magic [5]	LQ2-magic [1]	LQ1-data [1]	dummy [26]	LQ1-data [0]
LQ2-magic [3]	LQ1-data [3]	LQ2-magic [6]	dummy [33]	LQ2-magic [4]	LQ1-data [4]	LQ2-magic [0]
dummy [0]	dummy [29]	dummy [41]	dummy [14]	dummy [38]	dummy [47]	LQ2-magic [2]
dummy [31]	dummy [42]	dummy [9]	dummy [55]	dummy [5]	dummy [46]	dummy [34]
dummy [30]	dummy [20]	dummy [24]	dummy [17]	dummy [52]	dummy [1]	dummy [13]
dummy [3]	dummy [36]	dummy [40]	dummy [6]	dummy [8]	dummy [27]	dummy [48]
dummy [4]	dummy [23]	dummy [2]	dummy [7]	dummy [54]	dummy [12]	dummy [44]

(b) Step 13

dummy [22]	dummy [37]	dummy [16]	dummy [50]	dummy [11]	dummy [35]	dummy [39]
dummy [10]	dummy [25]	LQ1-data [5]	dummy [45]	dummy [19]	dummy [28]	LQ1-data [2]
dummy [51]	dummy [43]	dummy [21]	dummy [49]	LQ1-data [1]	dummy [53]	dummy [32]
LQ1-data [6]	dummy [15]	LQ2-magic [5]	LQ2-magic [1]	dummy [18]	dummy [26]	LQ1-data [0]
LQ2-magic [3]	LQ1-data [3]	LQ2-magic [6]	dummy [33]	LQ2-magic [4]	LQ2-magic [0]	LQ1-data [4]
dummy [0]	dummy [29]	dummy [41]	dummy [14]	dummy [38]	dummy [47]	LQ2-magic [2]
dummy [31]	dummy [42]	dummy [9]	dummy [55]	dummy [5]	dummy [46]	dummy [34]
dummy [30]	dummy [20]	dummy [24]	dummy [17]	dummy [52]	dummy [1]	dummy [13]
dummy [3]	dummy [36]	dummy [40]	dummy [6]	dummy [8]	dummy [27]	dummy [48]
dummy [4]	dummy [23]	dummy [2]	dummy [7]	dummy [54]	dummy [12]	dummy [44]

(c) Step 14

Figure 36: The second part logical T gate operations for qubits arranged vertically: Logical S gate correction and *Move-Back*. Please compare the final mapping with the initial mapping (Figure 32 (a)). The positions of the data qubits are the same in both mappings, but the magic qubits are not. Note that the rectangles, hexagons and bi-directed arrow respectively indicate S , $PrepZ$, $MeasZ$ and $SWAP$ gates.

dummy [22]	dummy [37]	↔ LQ1-data [5]	dummy [50]	dummy [11]	↕	dummy [35]	↔ LQ1-data [2]
dummy [10]	dummy [25]	dummy [16]	dummy [45]	LQ1-data [1]	↕	dummy [28]	↕
dummy [51]	dummy [43]	↕	dummy [21]	dummy [49]	dummy [19]	dummy [53]	↕ LQ1-data [0]
LQ1-data [6]	LQ1-data [3]	↕	LQ2-magic [5]	LQ2-magic [1]	dummy [18]	dummy [26]	dummy [32]
LQ2-magic [3]	dummy [15]	LQ2-magic [6]	dummy [33]	LQ2-magic [4]	LQ2-magic [0]	LQ1-data [4]	
dummy [0]	dummy [29]	dummy [41]	dummy [14]	dummy [38]	dummy [47]	LQ2-magic [2]	
dummy [31]	dummy [42]	dummy [9]	dummy [55]	dummy [5]	dummy [46]	dummy [34]	
dummy [30]	dummy [20]	dummy [24]	dummy [17]	dummy [52]	dummy [1]	dummy [13]	
dummy [3]	dummy [36]	dummy [40]	dummy [6]	dummy [8]	dummy [27]	dummy [48]	
dummy [4]	dummy [23]	dummy [2]	dummy [7]	dummy [54]	dummy [12]	dummy [44]	

(a) Step 15

dummy [22]	↔ LQ1-data [5]	dummy [37]	dummy [50]	LQ1-data [1]	LQ1-data [2]	↕	dummy [35]	↕
dummy [10]	dummy [25]	↕	dummy [16]	dummy [45]	dummy [11]	↕	dummy [28]	↕ LQ1-data [0]
dummy [51]	LQ1-data [3]	↕	dummy [21]	dummy [49]	dummy [19]	dummy [53]	dummy [39]	
LQ1-data [6]	dummy [43]	LQ2-magic [5]	LQ2-magic [1]	dummy [18]	dummy [26]	dummy [32]		
LQ2-magic [3]	dummy [15]	LQ2-magic [6]	dummy [33]	LQ2-magic [4]	LQ2-magic [0]	LQ1-data [4]		
dummy [0]	dummy [29]	dummy [41]	dummy [14]	dummy [38]	dummy [47]	LQ2-magic [2]		
dummy [31]	dummy [42]	dummy [9]	dummy [55]	dummy [5]	dummy [46]	dummy [34]		
dummy [30]	dummy [20]	dummy [24]	dummy [17]	dummy [52]	dummy [1]	dummy [13]		
dummy [3]	dummy [36]	dummy [40]	dummy [6]	dummy [8]	dummy [27]	dummy [48]		
dummy [4]	dummy [23]	dummy [2]	dummy [7]	dummy [54]	dummy [12]	dummy [44]		

(b) Step 16

LQ1-data [5]	dummy [22]	↕	dummy [37]	dummy [50]	LQ1-data [1]	dummy [28]	↔ LQ1-data [0]
dummy [10]	LQ1-data [3]	↕	dummy [16]	dummy [45]	dummy [11]	LQ1-data [2]	↔
dummy [51]	dummy [25]	dummy [21]	dummy [49]	dummy [19]	dummy [53]	dummy [39]	
LQ1-data [6]	dummy [43]	LQ2-magic [5]	LQ2-magic [1]	dummy [18]	dummy [26]	dummy [32]	
LQ2-magic [3]	dummy [15]	LQ2-magic [6]	dummy [33]	LQ2-magic [4]	LQ2-magic [0]	LQ1-data [4]	
dummy [0]	dummy [29]	dummy [41]	dummy [14]	dummy [38]	dummy [47]	LQ2-magic [2]	
dummy [31]	dummy [42]	dummy [9]	dummy [55]	dummy [5]	dummy [46]	dummy [34]	
dummy [30]	dummy [20]	dummy [24]	dummy [17]	dummy [52]	dummy [1]	dummy [13]	
dummy [3]	dummy [36]	dummy [40]	dummy [6]	dummy [8]	dummy [27]	dummy [48]	
dummy [4]	dummy [23]	dummy [2]	dummy [7]	dummy [54]	dummy [12]	dummy [44]	

(c) Step 17

Figure 37: (Continued from Figure 36) The second part logical T gate operations for qubits arranged vertically: Logical S gate correction and *Move-Back*. Note that the rectangles, hexagons and bi-directed arrow respectively indicate S , $PrepZ$, $MeasZ$ and $SWAP$ gates.

LQ1-data[5]	LQ1-data[3]	dummy [37]	dummy [50]	LQ1-data[1]	LQ1-data[0]	dummy [28]
dummy [10]	dummy [22]	dummy [16]	dummy [45]	dummy [11]	dummy [35]	LQ1-data[2]
dummy [51]	dummy [25]	dummy [21]	dummy [49]	dummy [19]	dummy [53]	dummy [39]
LQ1-data[6]	dummy [43]	LQ2-magic [5]	LQ2-magic [1]	dummy [18]	dummy [26]	dummy [32]
LQ2-magic [3]	dummy [15]	LQ2-magic [6]	dummy [33]	LQ2-magic [4]	LQ2-magic [0]	LQ1-data[4]
dummy [0]	dummy [29]	dummy [41]	dummy [14]	dummy [38]	dummy [47]	LQ2-magic [2]
dummy [31]	dummy [42]	dummy [9]	dummy [55]	dummy [5]	dummy [46]	dummy [34]
dummy [30]	dummy [20]	dummy [24]	dummy [17]	dummy [52]	dummy [1]	dummy [13]
dummy [3]	dummy [36]	dummy [40]	dummy [6]	dummy [8]	dummy [27]	dummy [48]
dummy [4]	dummy [23]	dummy [2]	dummy [7]	dummy [54]	dummy [12]	dummy [44]

(a) Final Mapping

Figure 38: (Continued from Figure 37) The second part of logical T gate operations for qubits arranged vertically: Logical S gate correction and *Move-Back*. Please compare the final mapping with the initial mapping (Figure 32 (a)). The positions of the data qubits are the same in both mappings, but the magic qubits are not. Note that the rectangles, hexagons and bi-directed arrow respectively indicate S , $PrepZ$, $MeasZ$ and $SWAP$ gates.