

Stochastic thermodynamic bounds on logical circuit operation

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Using a thermodynamically consistent, mesoscopic model for modern complementary metal-oxide-semiconductor transistors, we study an array of logical circuits and explore how their function is constrained by recent thermodynamic uncertainty relations when operating near thermal energies. For a single NOT gate, we find operating direction-dependent dynamics, and an optimal trade-off between dissipated heat and operation time certainty. For a memory storage device, we find an exponential relationship between the memory retention time and energy required to sustain that memory state. For a clock, we find that the certainty in the cycle time is maximized at biasing voltages near thermal energy, as is the trade-off between this certainty and the heat dissipated per cycle. We demonstrate that a simple control mechanism for the clock leads to a monotonic increase in cycle time certainty with biasing voltage alleviating its degradation at large biasing voltages. These results provide a framework for assessing thermodynamic costs of realistic computing devices, allowing for circuits to be designed and controlled for thermodynamically optimal operation.

While semiconductor-based computational capacity [1, 2] and efficiency [3–5] has exhibited sustained exponential growth over the past century, continued adherence of these trends is being disrupted as feature sizes approach atomic length scales and energetic scales near those of thermal noise [4, 5]. At such small scales, computation has to reconcile with unavoidable noise[6, 7]. This noisy limit has been termed *thermodynamic computing* [8, 9] and requires the development of new principles to achieve robust and energy-efficient information processing [10–13]. In this letter, we explore fundamental limitations encountered when computing in this regime by showing how the function of realistic logical circuits is bounded by recent thermodynamic uncertainty relations[14, 15].

Building upon equilibrium thermodynamics-based limits on computing operations, such as Landauer’s limit on the cost of bit erasure [16], stochastic thermodynamics[17] provides a framework for exploring the inherent limits of logical circuit operations on small scales, far from equilibrium. Recent results like fluctuation theorems, thermodynamic uncertainty relationships, and speed limits [18–27] can be used to strengthen bounds on computation within the thermodynamic computing regime, provided a physically-consistent, stochastic model. Using a recently developed model for current complementary metal-oxide-semiconductor (CMOS) transistors,[28] we study the interplay between accuracy, speed, and heat dissipation of an array of computations performed near thermal energies, locating optimal trade-offs between thermodynamic and operational costs.

Model – Many conventional engineering approaches for characterizing the effects of noise on circuit operation rely on assumptions only valid near equilibrium or near specific operating conditions [29–32], guaranteeing neither thermodynamic consistency nor accuracy far from equilibrium[33]. To provide a more faithful description of stochastic circuits, we require models that obey local detailed balance and exhibit

shot noise [34], while accurately reproducing known circuit characteristics. Recently, several stochastic models for CMOS devices have been proposed[28, 35, 36], enabling the study of noisy circuits and the associated thermodynamic costs when operating these devices near thermal energies[37–39]. Here, we employ one such model[28] to study systems of inverters, or logical NOT gates, built from single electron tunnel junctions operating within the classical limit [40], and using a capacitive charging model for the readout voltage. This model meets the three criteria emphasized above and in principle can be parameterized directly from microscopic calculations, providing a link between circuit performance and the underlying materials properties.

As shown in Fig. 1 (a), each inverter contains an N-type and a P-type transistor, each modeled by the band energy of an electron in the transistor $\epsilon_N(V_{in})$ and $\epsilon_P(V_{in})$, respectively, with energy levels controlled by the inverter’s input voltage V_{in} . This form of ϵ_i is valid in the limit of high gate capacitance. We set $\epsilon_N = qV_{in}$ and $\epsilon_P = \frac{3}{2}qV_d - qV_{in}$ to reproduce the characteristic voltage transfer curve of an inverter where q is the unit of charge[28]. The transistors are connected to three electron reservoirs: a source connected to the N-type transistor with reference voltage $V_s = 0$, a drain connected to the P-type transistor with voltage $V_d > 0$ resulting in a cross-voltage, and an output gate connected to both transistors. While the source and drain are held fixed, the output gate voltage changes as electrons accumulate in the gate according to $dV_g/dt = -J_g(t)/C_g$, where J_g is the current of electrons into the gate and C_g is the gate capacitance [41].

The system evolves stochastically according to a Markovian master equation $\partial_t \mathbf{P}(t) = \mathbf{W}\mathbf{P}(t)$ where \mathbf{P} is the configurational probability vector and \mathbf{W} is the stochastic generator, with elements W_{ij} specifying the rate at which an electron transitions from state j to i and $P_i(t)$ being the probability of being in state i at time t . The ratio of forward and reverse rates satisfy local detailed balance, $W_{ij}/W_{ji} = e^{-\beta(E_i - E_j)}$, where E_i

is the energy of a given configuration and $\beta = 1/k_B T$ is the inverse temperature defined with Boltzmann's constant k_B and temperature T . The rates are defined using the Fermi distribution where the transition rate of an electron from an electrode j to a transistor i is $W_{ij} = \Gamma (e^{\beta(\epsilon_i - qV_j)} + 1)^{-1}$ and the reverse is $W_{ji} = \Gamma - \Gamma (e^{\beta(\epsilon_i - qV_j)} + 1)^{-1}$ where Γ specifies the timescale for transitions and is physically set by the resistance of the transistor-electrode interface.

We work in units of thermal voltages and times, $V_T = k_B T/q$ and $\beta\hbar$ respectively, and set $\Gamma^{-1} = 5\beta\hbar$ so the timescale of electron transitions is longer than the timescale of thermal fluctuations [40], with \hbar being Planck's constant. For reference, at room temperature $V_T \approx 26$ meV and $\beta\hbar \approx 25$ fs. In these units, the model inverter is determined by a specification of the input voltage V_{in} and cross-voltage V_d .

Inverter – We start by considering the operation of a single NOT gate, which takes an input binary signal X and outputs its logical inverse Y according to the mapping:

$$X = \begin{cases} 0, & V_{in} = 0 \\ 1, & V_{in} = V_d \end{cases}, \quad Y = \begin{cases} 0, & V_{out} \leq \alpha V_d \\ 1, & V_{out} \geq (1 - \alpha)V_d \\ \emptyset, & \text{otherwise} \end{cases} \quad (1)$$

In the deterministic limit, when the input is $X = 1$, current through the P-type transistor is inhibited, bringing the capacitor gate into effective contact with only the source reservoir with $Y = 0$. Conversely, when the input voltage is $X = 0$, current is inhibited in the other transistor and the capacitor is connected to the drain reservoir, with $Y = 1$. All calculations performed for the single inverter are obtained using numerically exact time evolution, obtained using a Padé approximation [42] with a truncated Hilbert space of $16C_g(V_d + 4)$. For calculations where simulation times are not explicitly shown, we use time steps distributed logarithmically up to $10^{16}\beta\hbar$.

Figure 1(b) shows the time dependent response of the inverter to an alternating input voltage, with the left and right panels corresponding to setting $X = 0$ and $X = 1$, respectively at $t = 0$. Lower cross-voltages require less electron accumulation in the capacitor gate, and additionally fluctuations in the gate output are significantly larger for smaller V_d . These small accumulations and large fluctuations lead to response times that are orders of magnitude faster at low cross-voltages, highlighting a trade-off between output certainty and characteristic response time. While the steady-state statistics of the charged and discharged inverter are symmetric, we observe that the dynamics are not. As accentuated at larger V_d , the capacitor discharging happens rapidly, while charging occurs relatively slowly. This difference can be understood energetically. When discharging the capacitor, its occupation regulates the voltage in such a way that discharging becomes energetically more favorable as the gate empties. In the opposite direction, the accumulation of electrons becomes more energetically unfavorable as the gate charges, causing an exponential slowing of current into the gate as a function of time. Additionally, this leads to circulation of electrons between the

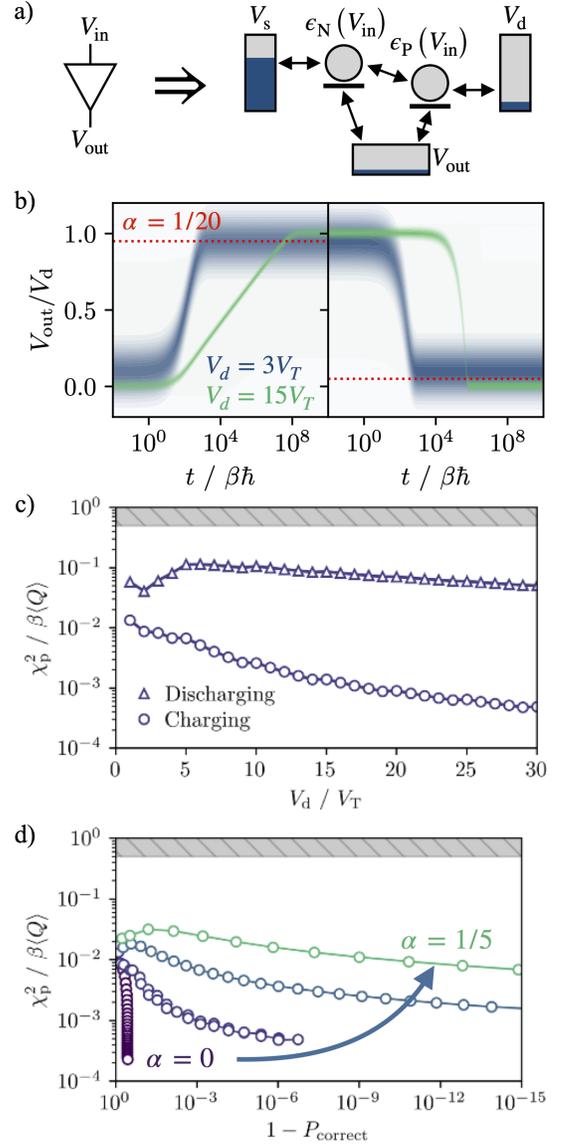


FIG. 1. Characterization of the NOT gate. (a) Illustration of the logical symbol and corresponding Markov model. (b) The probability of V_{out} with blue and green shading corresponding to different cross-voltages. The left (right) panel illustrate the dynamics of charging (discharging) the inverter, with input voltages switched at $t = 0$. (c) Trade-off between first passage time certainty and heat dissipation for discharging and charging over a range of V_d with $\alpha = 0.05$, with the shaded region forbidden by the thermodynamic uncertainty relation. (d) The same trade-off as in (c) for the charging process shown as a function of the probability of a correct gate output in the steady-state with varying accuracy thresholds $\alpha \in [0, 0.05, 0.1, 0.2]$.

transistors and capacitor when charging, while electrons move directly from the capacitor out of the inverter when discharging. The functionally unnecessary transitions caused by this circulation cause higher heat dissipation rates during the loading process.

To understand more precisely the interplay between the thermodynamic and operational costs for the inverter, we can

employ a thermodynamic uncertainty relationship

$$\chi_p^2 = \frac{\langle \tau_p \rangle^2}{\langle \delta \tau_p^2 \rangle} \leq \frac{\langle Q \rangle}{2qV_T} \quad (2)$$

where brackets indicate an trajectory ensemble average, τ_p is the first passage time to an output voltage passing the accuracy threshold α [43], and $\delta x = (x - \langle x \rangle)$ [44]. The thermodynamic uncertainty relationship is a general result from stochastic thermodynamics, valid for any Markovian jump process. It states that the certainty in the first passage time, χ_p , is bounded from above by the heat dissipated over a trajectory, Q , defined as $Q = \int_0^{\tau_p} dt \dot{Q}(t)$, with $\dot{Q}(t) = \sum_{i,j} W_{ij} P_j(t) \ln W_{ji}/W_{ij}$ [45]. The bound relates the minimum thermodynamic cost for a given desired certainty in the first passage time. In practical terms, higher certainty in operation time allows for processing input bits at higher rates with lower probabilities of incorrect or inconclusive readings, while reducing excess dissipated heat caused by longer operating times. Figure 1 (c) shows how this bound depends on the cross-voltage. For the discharging process, we observe an optimal compromise between first passage time certainty and heat dissipation near $V_d = 5V_T$. No such peak is immediately evident for the charging process and, more strikingly, the bound is significantly looser due to larger fluctuations in first passage times and the excess dissipated heat caused by internal cycle currents. That the bound is not saturated for any V_d implies that the operation of the NOT gate is not limited by thermodynamic constraints and that observed limits are products of the particular CMOS design and operation.

In Fig. 1 (d), we vary the cross-voltage and plot the trade-off between first passage time certainty and heat dissipation, as a function of the probability of a correct output at long times $P_{\text{correct}} = \langle Y \rangle_{X=0}$, where the ensemble average is over long-time trajectories with the specified input. We additionally show multiple curves corresponding to differing values of α and observe the emergence of an optimal trade-off, near $V_d = 3$. Loosening α moves the curves significantly towards the bound by dissipating less heat. The combination of these effects allows for thermodynamically optimal operation at higher probabilities of correct outputs as α increases, with similar but less pronounced effects not shown for the discharging process.

Memory Device – Next we consider a static random access memory (SRAM) device built by coupling two inverters, as shown in the inset of Fig. 2 (a). This device operates using so-called flip-flop circuitry, meaning it exhibits a bistable steady-state, which is a dynamical consequence of a pitchfork bifurcation. The inverter's state can be set by switching on V_{set}^1 , employing feedback from V_{out}^1 to V_{in}^2 . Here, we will focus on memory maintenance, which can be reliably achieved at sufficiently large cross-voltages by switching both setting voltages off and both feedback loops on. To simulate the memory device, we perform an approximate evolution using a fourth-order Runge-Kutta scheme acting on a truncated Hilbert space using a time step of $\Delta t = \beta\hbar/10$ until a final

time of $t_f \approx 10^6 \beta\hbar$.

Figure 2 (a) shows the steady-state probability of observing an output voltage $V_{\text{out}} = V_1^{\text{out}}$. The requisite bistability for memory storage arises at $V_d/V_T \approx 2.5$ where the cross-voltage overcomes the effects of thermal fluctuations. Notably the bistability is a unique consequence of the nonequilibrium driving, which disappears in the absence of a finite cross-voltage. At finite V_d , the degeneracy of the steady-state manifests as a spontaneous switching of V_{out} as a function of time, illustrated in Fig. 2 (a), as evaluated using Gillespie simulations [46]. For large V_d we observe V_{out}/V_d is localized near 0 or 1 for time scales much larger than individual inverter operation time scales $\langle \tau_p \rangle$, indicating persistent memory storage. At long times, however, output voltage is stochastically inverted, corrupting the memory storage.

We define τ_{err} as the time required for a memory device, initialized in one of the bistable states, to experience a bit flip memory error. Figure 2 (b) shows the average time required for a bit flip to occur $\langle \tau_{\text{err}} \rangle$ [47] as a function of the characteristic time of a single inverter. We observe that the rate

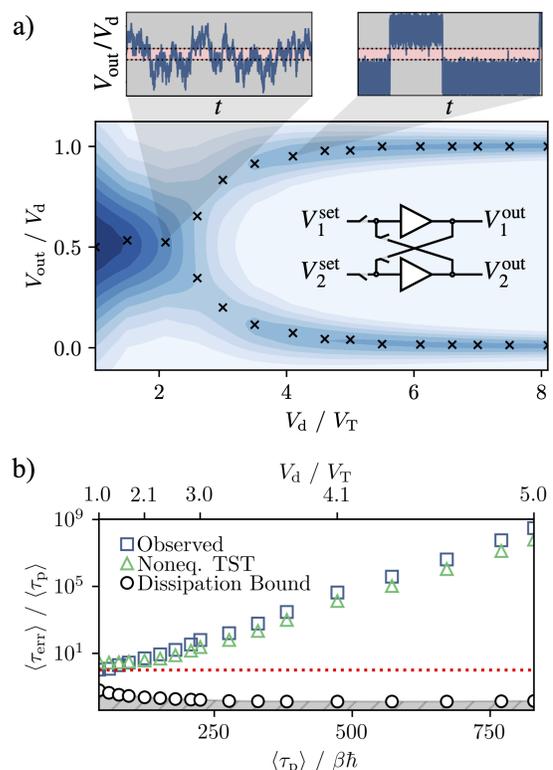


FIG. 2. Characterization of the memory device's behavior and adherence to thermodynamic speed limits. (a) Probability of V_{out} as a function of V_d , with crosses locating points of maximum probability at each V_d illustrating the onset of bistability. Example trajectories are shown for before and after the onset of bistability. (b) Mean time for a memory error as a function of the inverter relaxation time, controlled by increasing V_d , as indicated on the top x-axis label, with the red dashed line indicating $\langle \tau_{\text{err}} \rangle = \langle \tau_p \rangle$. The shaded region is forbidden by the dissipation time uncertainty principle.

of memory error occurrences decreases exponentially with respect to $\langle \tau_p \rangle$, thus increasing the average memory stability time by roughly five orders of magnitude, from about 100 ns to 20 ms for $V_d/V_T = 2$ to 5. The dissipation time uncertainty principle [21] puts a lower bound on the average time for a bit flip memory error to occur

$$\langle \tau_{\text{err}} \rangle \geq (\beta \langle \dot{Q} \rangle)^{-1} \quad (3)$$

where $\langle \dot{Q} \rangle$ is the average rate of heat dissipation in the steady-state. The region restricted by this lower bound is shown as the shaded area in Fig. 2 (b), indicating that the inequality is satisfied, but far from saturated. This suggests that energy pumped into the SRAM device is efficiently directed into preserving the memory state. Indeed this can be quantified using a nonequilibrium version of transition state theory[23]. Transition state theory bounds the rate of a transition between two metastable states using the stationary distribution $P_{\text{ss}}(V_{\text{out}})$ and an uncorrelated estimate of the time to cross a dividing surface between the two states. Taking the dividing surface to be $V_{\text{out}} = V_d/2$, and the typical time to cross the barrier as $\langle \tau_p \rangle$, a nonequilibrium transition state theory estimate for $\langle \tau_{\text{err}} \rangle$ is

$$\langle \tau_{\text{err}} \rangle \gtrsim \langle \tau_p \rangle \frac{P_{\text{ss}}(V_{\text{out}}/V_d \leq \alpha)}{P_{\text{ss}}(V_{\text{out}}/V_d = 1/2)} \quad (4)$$

which is shown in Fig. 2 (b). Here the steady-state has been evaluated numerically with $\alpha = 0.4$. The nonequilibrium transition state theory provides a very accurate estimate of the memory time, reflecting the likelihood of observing a fluctuation of $V_{\text{out}} = 1/2$ as becoming exponentially unlikely with increasing V_d in accord with recent large deviation function analysis[37]. The accuracy of the transition state theory estimate demonstrates that little energy is wasted speeding up transitions[23].

Clock – An uneven number of inverters coupled sequentially in a ring creates a system with a frustrated steady-state, because all inverters cannot simultaneously output the logical inverses of their inputs. This frustration causes cyclic oscillations, whose period is controlled by inverter operation times, making the device operate as a clock under deterministic conditions and providing an example of circuitry with non-trivial functionality. To simulate the dynamics of such a clock, we perform kinetic Monte Carlo simulations using the Gillespie algorithm. We define the time for the clock to undergo a single cycle τ_c as the time for the output, Y , to cycle from $1 - \alpha$ to α and back again to $1 - \alpha$, using $\alpha = 0.4$. All results are averaged over simulations containing at least 50,000 clock cycles.

In Fig. 3 (a), we show the output voltage autocorrelation function $C_{V_i, V_i}(t) = \langle \delta V_i(0) \delta V_i(t) \rangle$, as a function of time and cross-voltage. At low cross-voltages, the three output voltages evolve nearly independently, with $C_{V_i, V_i}(t)$ revealing exponential correlations. Above $V_d \approx 3V_T$ persistent oscillations emerge but are damped by the stochasticity of the evolution. We find a maximal persistence in the autocorrelation function oscillation at $V_d \approx 7V_T$, where the clock undergoes approximately 3.5 cycles. In this region oscillations are persistent

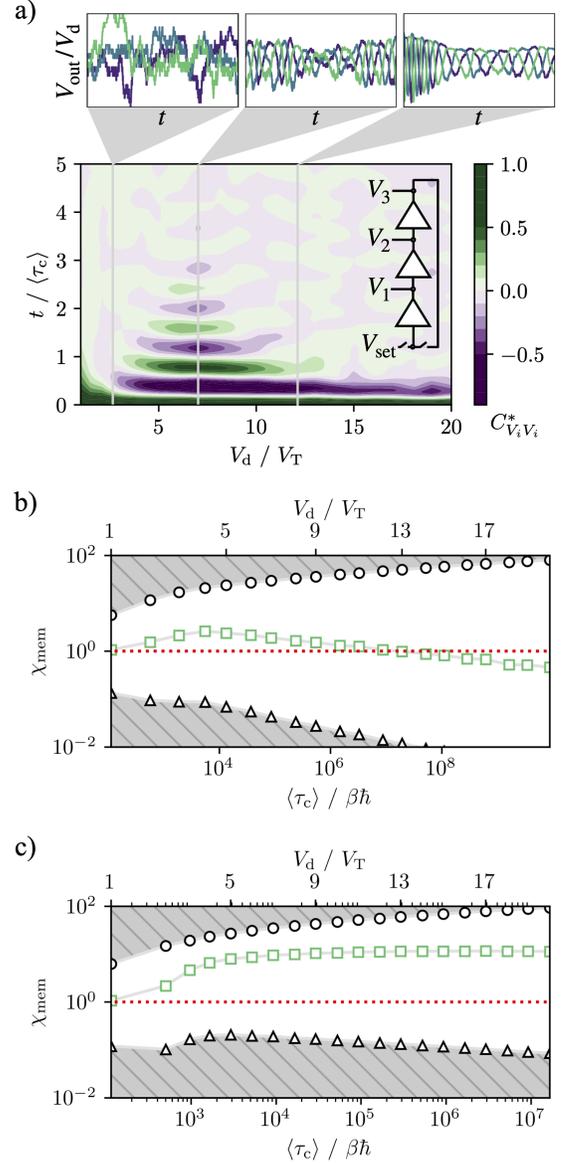


FIG. 3. Adherence to thermodynamic bounds of the logical clock. (a) Rescaled voltage autocorrelation function $C_{V_i, V_i}^*(t) = C_{V_i, V_i}(t)/C_{V_i, V_i}(0)$ as a function of applied cross-voltage. Example trajectories at $V_d = [2.1V_T, 7V_T, 12.1V_T]$, with each curve representing how the output voltage of one of the inverters evolves. (b) The certainty in clock operation time χ_{mem} as a function of average clock cycle time $\langle \tau_c \rangle$ and applied cross-voltage (top axis) (green squares), with the shaded regions indicating the forbidden regions from the uncertainty relations. The red dashed line indicates where $\langle \tau_c \rangle^2 = \langle \delta \tau_c^2 \rangle$. (c) The certainty in clock operation as in (b) with the simplest threshold control mechanism.

for long times and the fluctuations in τ_c are small relative to the mean cycle time. Above $V_d \approx 10V_T$, the autocorrelation exhibits oscillation for only 1/2 of a cycle because, while oscillations are persistent for long times, the fluctuations in τ_c are large relative to the mean cycle time as anticipated from Fig. 1 (c) and the single NOT gate. In this regime, we find

the cycle time to be inversely proportional to voltage output amplitude, which evolves stochastically.

We define the certainty in the cycle time as $\chi_{\text{mem}} = \sqrt{\langle \tau_c \rangle^2 / \langle \delta \tau_c^2 \rangle}$, and plot this for $V_d \in [1V_T, 20V_T]$ in Fig. 3 (b). The red dashed line indicates where the cycle time's fluctuations are equal to its mean, where we find a narrow range of cross-voltages where there is reliable cycling. The thermodynamic uncertainty relationships expressed in Eqs. 2 and 3 can be adapted to give upper and lower bounds on this quantity

$$\sqrt{\frac{\langle Q \rangle}{2}} \geq \chi_{\text{mem}} \geq \sqrt{\frac{\langle \tau_c \rangle}{\beta \langle \dot{Q} \rangle \langle \delta \tau_c^2 \rangle}}, \quad (5)$$

where $\langle Q \rangle$ is the average heat dissipated over a cycle, and $\langle \dot{Q} \rangle$ is the average rate of heat dissipation in the steady-state. The upper and lower bounds are shown as the shaded regions in Fig. 3 (b), showing that the upper bound is best saturated when χ_{mem} is maximized. This occurs for a large enough cross-voltage that the coupled inverters exhibit bistability, but not so large that the fluctuations in the transition time are large.

To expand the range of reliable cycle times, we propose a simple control mechanism acting between each of the inverters. If the output voltage from an inverter is greater than $1 - \alpha$, then a thresholding mechanism exerts work on the system and provides an input voltage of exactly V_d to the next inverter in the cycle, with an analogous threshold setting the input to 0 if the output is less than α . By doing this, the inverter is always driven with an optimal input voltage amplitude, circumventing the slow response observed when voltage amplitudes are small. Figure 3 (c) shows the resulting performance of χ_{mem} . As the cross-voltage increases, χ_{mem} increases monotonically, avoiding the loss in cycle time certainty at large cross-voltages, plateauing to provide constant clock reliability across a broad range of cycle times. The uncertainty relationships continue to be best saturated at intermediate values of V_d , indicating optimal heat dissipation costs for cycle certainty remains in a similar range as without control.

Conclusion – We have used a Markovian model for realistic logical inverters in the regime of thermodynamic computing to explore the interplay between operating characteristics, like accuracy and time, and thermodynamic properties, particularly heat dissipation. Our results demonstrate the theoretical limits of CMOS circuits using bounds derived from stochastic thermodynamics. As we have shown, this provides a framework for simultaneously exploring the fundamental behavior of noisy computational circuits, characterizing their optimality, and using the gained insight to propose more efficient operating procedures and circuits. We expect this work will provide a foundation for future work towards understanding and designing efficient thermodynamic computers. Current techniques should allow for the improvement of thermodynamic efficiencies by adapting principles from optimal control theory to operational control schemes [48–53] and by exploring the effects of circuit layout [13]. To extend this approach to larger circuits, more scalable simulation techniques, such as tensor network methods [54–58], can be adapted.

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Data availability – The source code for the calculations done and all data presented in this work are openly available on Zenodo at <https://doi.org/10.5281/zenodo.7251316> [59].

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