

Low-damage electron beam lithography for nanostructures on Bi_2Te_3 -class topological insulator thin films

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Nanostructured topological insulators (TIs) have the potential to impact a wide array of condensed matter physics topics, ranging from Majorana physics to spintronics. However, the most common TI materials, the Bi_2Se_3 family, are easily damaged during nanofabrication of devices. In this paper, we show that electron beam lithography performed with a 30 or 50 kV accelerating voltage – common for nanopatterning in academic facilities – damages both nonmagnetic TIs and their magnetically-doped counterparts at unacceptable levels. We additionally demonstrate that electron beam lithography with a 10 kV accelerating voltage produces minimal damage detectable through low-temperature electronic transport. Although reduced accelerating voltages present challenges in creating fine features, we show that with careful choice of processing parameters, particularly the resist, 100 nm features are reliably achievable.

INTRODUCTION

The discovery of topological insulators (TIs) has introduced exciting new directions in condensed matter physics, including dissipationless edge conduction without an applied magnetic field [1, 2], new platforms for spintronics [3–5], and even the possibility of Majorana fermions, which have been proposed as a basis for qubits [6, 7]. The tetradymites Bi_2Se_3 , Sb_2Te_3 , and Bi_2Te_3 were among the first topological insulators predicted theoretically [8]. Successful thin film growth of these materials and experimental confirmation of their hallmark spin-momentum-locked, massless Dirac dispersion soon followed [8, 9]. Tuning the Fermi level was achieved by alloying Bi and Sb on cation sites, and in some cases Te and Se on the anion sites, to form materials like $(\text{Bi, Sb})_2\text{Te}_3$ (BST) [10] and $(\text{Bi, Sb})_2(\text{Te, Se})_3$ (BSTS) [11]. The ability to position the Fermi level at or near the Dirac point, where physics related to the topological surface states is most visible, along

with demonstration of the quantum anomalous Hall effect in magnetically doped compounds of BST [1, 12], has made BST and BSTS some of the most widely studied TI materials in the field.

However, starting with carefully optimized as-grown films does not guarantee fabricated devices will retain the original film’s electronic qualities. The BST family is known to be easily damaged during processing. For example, tellurium can evaporate from the film if processing temperatures are not kept low. Furthermore, tellurium will preferentially oxidize upon prolonged air exposure or oxygen plasma cleaning [13–15]. Nonetheless, many interesting micron-scale devices have been produced using careful choice of processing parameters [2, 3, 16].

Scaling device features to the nanoscale – critical for exploration of Majorana physics, for example – introduces new challenges. To pattern features below a few microns, most academic fabrication facilities use electron beam lithography (EBL) with

25-100 kV accelerating voltages. It has been standard to use such tools for TI nanostructures [17–27], although some EBL-free alternative methods have been proposed [28]. In this paper we demonstrate that 30 and 50 kV accelerating voltages cause unacceptable damage to TI thin films. We also show that EBL with lower-energy 10 kV electron beams does not significantly change the electronic properties of TI films. Unfortunately, lower-energy EBL makes it difficult to reliably produce features on the order of 100 nm because of strong small-angle scattering of electrons passing through the resist. We provide guidance for generating 100 nm features in a liftoff-based fabrication scheme. Combining our guidance with other recommendations to reduce fabrication-related damage in TI devices [29] can enable production of nanostructured devices with minimal electrical sample degradation [30, 31].

METHODS

2.1 MATERIALS GROWTH

Three different materials were used in this paper. Film 1 was composed of 8 quintuple layer (QL) $(\text{Bi}_{0.5}\text{Sb}_{0.5})_2\text{Te}_3$; both Film 2 and Film 3 were composed of 6 QL $(\text{Cr}_{0.12}\text{Bi}_{0.26}\text{Sb}_{0.62})_2\text{Te}_3$. All three films were grown on epi-ready semi-insulating GaAs (111)B substrates in an ultra-high vacuum Perkin-Elmer molecular beam epitaxy (MBE) system. Before growth, the substrates were loaded into the MBE chamber and pre-annealed at a temperature of 670°C in a Te-rich environment to remove the oxide on the surface. During growth of Film 1, high-purity Bi, Sb and Te were evaporated from standard Knudsen cells respectively. The substrate was kept at 215°C . During growth of Films 2 and 3, high-purity Cr, Bi, Sb and Te were evaporated from standard Knudsen cells respectively. The substrate was kept at 200°C .

2.2 HALL BAR FABRICATION AND MEASUREMENT

To study the effect of electron beam exposure on electronic transport in BST and chromium-doped, magnetically-ordered BST (Cr-BST), devices were fabricated on two chips of Film 1 (BST) and one chip of Film 2 (Cr-BST). Devices consisted of long Hall bars with six, eight, or ten voltage contacts on each of the top and bottom edge. As shown in Figure 1,

regions of the device mesa probed by two sets of contact pairs were locally exposed to electron beams; this enabled longitudinal and Hall transport measurements of isolated regions of each Hall bar. Between the two BST chips, three long Hall bars—each with three quartets of longitudinal and transverse contact pairs—were fabricated (Figure S1). The Cr-BST chip featured two long Hall bars, one with four and one with five quartets of contact pairs (Figure S2). On the BST chips, three regions of the BST material were left unexposed to electron beams; four regions were exposed with doses ranging $100\text{--}200\ \mu\text{C}/\text{cm}^2$ with a 10 kV accelerating voltage; two regions were exposed with 300 or $600\ \mu\text{C}/\text{cm}^2$ doses with a 30 kV accelerating voltage. On the Cr-BST chip, a total of two Cr-BST regions were left unexposed to electron beams; five regions were exposed at 10 kV with doses that ranged from $100\text{--}1,000\ \mu\text{C}/\text{cm}^2$; two regions were exposed at 50 kV with $500\ \mu\text{C}/\text{cm}^2$ and $2,500\ \mu\text{C}/\text{cm}^2$ doses. Higher exposure doses were selected at higher accelerating voltages to account for the larger clearing dose for resist at these voltages, due in turn to the lower scattering cross sections at higher accelerating voltages. Specific accelerating voltages were chosen based on the capabilities of the tools employed for patterning [32].

Devices on all chips were fabricated as follows: first, photolithography and argon ion milling were used to define device mesas on the as-grown BST or Cr-BST film. Next, Ti/Au contacts were added using photolithography, electron beam (e-beam) metal evaporation, and liftoff. Each chip was then again coated with polymer resist, in this case poly(methyl methacrylate) (PMMA), commonly used for electron beam lithography. Isolated regions of the Hall bars were then exposed to electron beams to simulate the exposure that would occur during electron-beam lithography. Device micrographs taken at this point in the fabrication process are shown in the supplemental materials (Figures S1, S2). Electrostatic gates were then added to the Cr-BST devices as follows: After removing the PMMA with a solvent rinse and globally depositing a 1 nm aluminum seed layer with e-beam evaporation, 40 nm of alumina was deposited globally using atomic layer deposition to act as a gate dielectric. Photolithography, e-beam evaporation, and liftoff were used to define the metallic top gate. Finally, another photolithography step defined

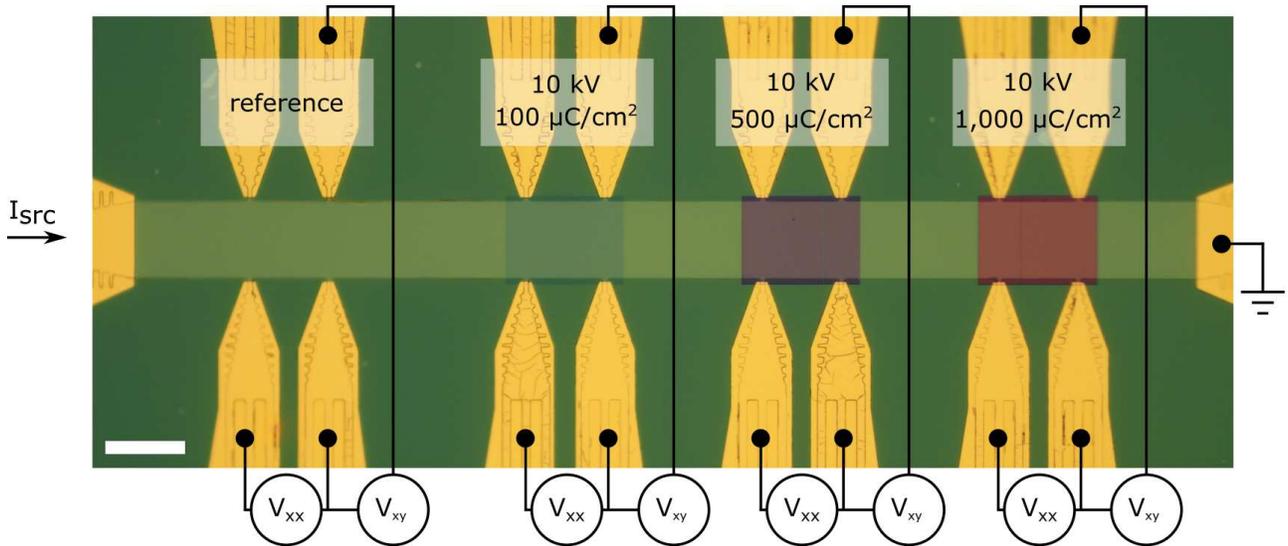


Fig. 1: Optical image of a Hall bar device fabricated on Film 2, taken immediately after the device was exposed to electron beams with the undeveloped resist still in place. Contacts on the left and right side of the device were used to source (I_{src}) and drain current. Four quartets of contact pairs allow longitudinal (V_{xx}) and Hall (V_{xy}) voltage measurements of four isolated regions of the Cr-BST Hall bar. These four isolated regions were either left unexposed to electron beams (reference region) or exposed with a 10 kV electron beam at various doses, as indicated. Due to changes in the optical properties of PMMA after exposure, regions exposed to electron beams are visible as the colored rectangles over the device mesa. Scale bar: 80 μm .

a mask through which alumina covering the contact pads was removed by a wet etch. Standard low-frequency electronic transport measurements of the BST (Cr-BST) Hall bars were performed at a base temperature of 1.55 K (30 mK).

Throughout the fabrication process, care was taken to avoid thermal or chemical damage to the native Cr-BST and BST films. As noted in literature surrounding fabrication of HgTe devices [33, 34], standard processing temperatures can impact the quality of fragile topological materials. Following past work with BST and Cr-BST [16, 30, 35–37], all photo- and e-beam resist bakes were performed at 80° C, not 120-180° C as is typical for resist bakes on less fragile substrates. Full details of the fabrication procedure and electrical measurements, as well as discussion of processing differences between the BST and Cr-BST chips, can be found in the supplemental materials.

2.3 POINT SPREAD FUNCTION SIMULATIONS

Point spread functions (PSFs) describe the spatial pattern of energy density deposited into a par-

ticular resist/sample/substrate stack after exposure to an electron beam point source. PSFs shown in Figure 4(a,b) and in the supplemental materials were simulated with the GenISys TRACER Monte Carlo simulation tool. The stack through which electron trajectories were simulated included, from the top down: (1) 150 nm PMMA (2) 8 nm Sb_2Te_3 (3) 0.5 mm GaAs. The electron injection energy was fixed at the accelerating voltage times one electron charge. For each accelerating voltage, one million trajectories were simulated.

2.4 LITHOGRAPHY TESTS

Demonstrations of 100 nm features patterned by 10 kV EBL were performed on four chips cut from the Cr-BST Film 3 and on two chips of bare GaAs. Each chip was cleaned with acetone and isopropanol rinses. After cleaning, each chip was spun at 4000 rpm with a PMMA resist and baked at 80° C. Resist specifications and bake times are listed in Table 1. After baking, all four chips were loaded together into a Raith VOYAGER electron beam lithography system. Exposures were performed with a

10 kV beam accelerating voltage and a 66.9 pA beam current. A 5 nm step size was used for area writes. For writes of single-pixel lines (SPLs), either 3, 5, or 8 nm step sizes were used [32]. Patterns on the Cr-BST film targeted thin exposed lines as well as the inverse pattern of thin resist bridges - where two large areas are written as close as possible to one another while leaving some resist unexposed between them. On the GaAs chips, writes targeted the same goals, but were extended laterally over 1 mm to enable cleaving across the key features to image resist profiles.

After exposure, Cr-BST and GaAs chips were developed at ambient temperature with 55 s 1:3 methyl isobutyl ketone:isopropanol / 20 s isopropanol and immediately blown dry. Exposed regions of the Cr-BST chips were then metallized with 50 nm e-beam-evaporated Al after a 10 s *in situ* Ar ion etch, followed by liftoff in acetone with sonication. The GaAs chips were instead sputter coated with 4.5 nm 60/40 Au/Pd and then cleaved across the features of interest [32]. Scanning electron micrographs were then taken of all samples. The Cr-BST samples were imaged top-down to extract the horizontal length scales of the critical features; GaAs samples were imaged at an angle to view cross-sectional resist profiles.

RESULTS AND DISCUSSION

3.1 ELECTRON BEAM-INDUCED DAMAGE TO TOPOLOGICAL INSULATOR FILMS

Electron beam exposures are described by an accelerating voltage, used to accelerate electrons towards the sample, and a charge dose, describing the electron fluence that crosses the surface of the sample's resist. The clearing dose describes the electron fluence necessary to fully expose a given resist stack, meaning that the exposed region of resist will be fully dissolved during development, and is typically the minimum dose needed for a successful EBL exposure. The magnitude of the clearing dose is determined by the resist thickness, how strongly the electron beam interacts with the resist, and any back-scattering off of the sample, which effectively increases the electron flux through the resist. Clearing dose can also be affected by choice of development conditions. Throughout this

work, we use the developer 1:3 methyl isobutyl ketone:isopropanol/isopropanol. The clearing dose tends to increase roughly linearly with accelerating voltage since scattering cross-sections decrease as the electron beam energy increases.

Although electron beams can be extremely narrow (~ 8 nm) as they enter a sample's resist coating, they scatter and spread out as they pass through the resist and into the sample below. This broadening causes proximity effects, by which the effective dose is higher towards the center of large area writes due to overlap between adjacent exposures. In contrast, near corners and edges, as well as in very thin or single-pixel line writes, the effective dose is reduced since there are fewer adjacent points exposed. As a result of these proximity effects, the doses required for thin lines or near corners and edges can be much higher than clearing doses in the center of large area writes.

As discussed above, to study the effects of electron beam exposure on nonmagnetic TIs, several Hall bars were fabricated on a BST film (Film 1). Density n and mobility μ of each locally exposed region were extracted from Hall and longitudinal resistance measurements at $T \approx 1.5$ K. As shown in Figure 2(a,b), for exposure at either 10 kV or 30 kV the density increased (indicating electron doping) and the mobility decreased (indicating increased disorder) as the dose of electrons was increased. However, exposures at 10 kV caused substantial deviations from the reference unexposed regions only at doses higher than the clearing dose. In contrast, regions exposed at 30 kV exhibited substantial density increases and mobility decreases even at the clearing dose. These data indicate that clearing dose exposures at 10 kV only minimally perturb electronic transport behavior in BST, whereas exposures at 30 kV significantly degrade the material.

As discussed above, Hall bars with local electron beam exposure were also fabricated on a Cr-BST chip (Film 2). Magnetically-doped TIs, including Cr-BST, are known to host the quantum anomalous Hall effect (QAHE), a zero-magnetic-field analog of the quantum Hall effect [1, 12]. Ferromagnetic order of the dopants breaks time reversal symmetry and opens a gap in the Dirac surface state of the TI. When the Fermi level is tuned to lie within this mass gap, the QAHE is observed. In electrical trans-

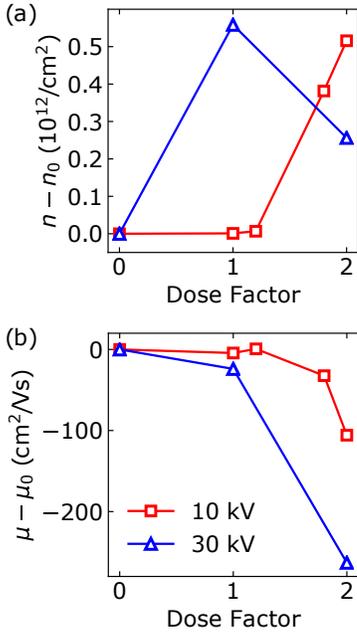


Fig. 2: Effects of electron beam exposure on non-magnetic TIs. Changes in (a) density and (b) mobility relative to a reference region unexposed to electron beams. Data are shown as a function of the dose factor, the ratio of the exposure dose to the clearing dose. For 10 kV exposures (red squares) the clearing dose is $100 \mu\text{C}/\text{cm}^2$, and exposures range from 0-200 $\mu\text{C}/\text{cm}^2$. For 30 kV exposures (blue triangles) the clearing dose is $300 \mu\text{C}/\text{cm}^2$, and exposures range from 0-600 $\mu\text{C}/\text{cm}^2$. Raw data are presented in Figure S3.

port measurements the QAHE is seen as a vanishing longitudinal conductivity, $\sigma_{xx} = 0$, and a quantized Hall conductivity, $\sigma_{yx} = \pm e^2/h$, whose sign is dependent on the Chern number $C = \pm 1$ and tuned by the out-of-plane orientation of the sample's magnetization. A quantized value of the conductivity tensor ($\sigma_{yx} = \pm e^2/h$, $\sigma_{xx} = 0$) corresponds to complete magnetization of the sample in the positive or negative out-of-plane direction and the corresponding Chern number $C = \pm 1$.

After magnetizing the Cr-BST sample in a 0.5 T magnetic field normal to the plane of the device and tuning the Fermi level to the center of the magnetic exchange gap via electrostatic gating, the QAHE was observed for all devices, independent of electron beam exposure [32]. Figure 3(a) shows a typical QAHE hysteresis loop acquired for a region of

a Hall bar that was not exposed to electron beams as the magnetic field normal to the plane of the device is swept back and forth between -0.5 T and 0.5 T , well past the film's coercive field of 0.2 T . The left (red) axis plots the longitudinal conductivity $\sigma_{xx} = \rho_{xx}/(\rho_{xx}^2 + \rho_{yx}^2)$ which approaches $0 e^2/h$ away from the coercive field. The right (blue) axis plots the Hall conductivity $\sigma_{yx} = \rho_{yx}/(\rho_{xx}^2 + \rho_{yx}^2)$, which switches between $\sigma_{yx} = \pm e^2/h$ at the coercive field. Conductivities ($|\sigma_{yx}| < e^2/h$, $\sigma_{xx} > 0$) occur when the sample magnetization is not homogeneous and out-of-plane, and are observed as the magnetization reverses at external magnetic fields close to the coercive field $\pm 0.2 \text{ T}$. Figure 3(b) replots the data from (a) in a standard parametric plot of σ_{xx} against σ_{yx} , which visualizes the flow of the QAHE across the $C = \pm 1$ topological phase transition at magnetization reversal [35, 38].

When the magnetization is reversed in Cr-BST, one of two patterns is observed in conductivity measurements: (1) explicit tuning through a trivial insulating phase $C = 0$, which is characterized by $\sigma_{xx} \sim 0$, $\sigma_{yx} \sim 0$ (Figure 3(b,e)), and (2) directly tuning between $C = \pm 1$ without observable trivial insulating behavior [38–40]. Which of these two behaviors occurs is thought to correlate with the thickness of the Cr-BST film, possibly as a result of competition between the topologically nontrivial magnetic exchange gap and a topologically trivial gap formed by hybridization of surface states in films less than $\sim 6 \text{ nm}$ thick [38]. Fabrication techniques that alter a sample's behavior at the topological phase transition risk convoluting transport features of the physics of interest with damage-related phenomena or destroying them entirely. For example, proposals to study chiral Majorana edge modes at interfaces between quantum anomalous Hall and superconducting materials rely on careful control over a $C = \pm 1 \rightarrow C = 0$ phase transition [7, 41].

The behavior across the topological phase transition at this magnetization reversal was observed to evolve with both dose and accelerating voltage. As shown in the parametric plots of Figure 3, regions exposed with a 10 kV accelerating voltage maintain the same qualitative behavior as the reference region across magnetization reversal. However, regions exposed at 50 kV exhibit an asymmetric transition be-

tween magnetization orientations. This distinction between how the reference region and regions exposed at 50 kV pass through the topological phase transition at the coercive field can also be seen in the hysteresis loop of Figure 3(d), where the asymmetry in σ_{xx} across the coercive fields is responsible for the asymmetry in Figure 3(f). The behavior of the regions exposed at 50 kV represents a substantial deviation from the as-grown film behavior and is clear evidence of electron beam-induced damage. Data from additional regions of the Cr-BST Hall bars are presented in the supplemental materials.

Additionally, in areas exposed with a 10 kV accelerating voltage, the optimal gate voltage shifts nearly linearly with dose [32]. Since the optimal gate voltage reflects the doping and number of mid-gap states, this shift indicates that electron doping and/or population of defect states scales with the electron dose, as expected. Areas exposed at 50 kV did not display a monotonic relationship between dose and doping [32]. We speculate that this difference indicates that damage mechanisms are different at the different accelerating voltages, but further study is needed to clarify the relationship between dose and damage.

3.2 OPTIMIZING 10 kV ELECTRON-BEAM LITHOGRAPHY FOR 100 NM FEATURES

We have shown that damage to the Bi_2Te_3 family of materials during EBL significantly alters their electronic properties, but that this can be mostly avoided by using a 10 kV accelerating voltage. Yet patterning nanostructures at such a low accelerating voltage presents challenges. At standard accelerating voltages (25-100 kV), electrons undergo minimal small-angle forward scattering as they pass through the resist layer [32] and tend to pass straight through the resist [42–44]. In contrast, at 10 kV electrons undergo substantial small-angle forward scattering as they initially pass through the resist layer. As a result, the electron beam broadens considerably as it travels through the resist [42, 43, 45, 46].

Figure 4(a,b) shows simulations of energy density deposited into resist as a function of distance from the center of the electron beam at three different depths within a 150 nm PMMA resist layer. As shown in Figure 4(a), with a 50 kV accelerating voltage most of the energy is deposited within

10 nm of the center of the beam throughout the resist. With a 10 kV accelerating voltage, the energy is again deposited within about 10 nm laterally of the beam center at the top of the resist layer but within a much broader 100 nm lateral distance from the beam center near the bottom of the resist. This difference in beam broadening is marked by the red marker on the x-axes of Figures 4(a,b), which indicate the radius at which the energy density has dropped by a factor of ten relative to the energy density at the center of the beam at the surface of the Sb_2Te_3 (depth 142 nm). Insets in Figure 4(a,b) sketch resultant cross-sectional resist profiles after development. At 50 kV accelerating voltage, the deposited energy remains close to the center of the beam, therefore resist sidewalls remain vertical throughout the resist layer. At 10 kV, however, small-angle scattering causes the deposited energy to broaden as the beam passes through the resist, so the sidewalls taper away from the beam center. Figure 4(c) shows a scanning electron micrograph of a resist profile after exposing resist at 10 kV accelerating voltage, developing, and then depositing a thin metal layer to enhance image contrast; inwardly-slanted sidewalls are clearly visible.

Slanted sidewalls make ≤ 100 nm features challenging to produce with a 10 kV accelerating voltage. Narrow resist bridges can completely pinch off and delaminate close to the substrate [32]. Even if this does not occur, dramatic undercuts can reduce the mechanical stability of thin bridges. These issues limit resist choices to thinner layers. Unfortunately, thin resist limits subsequent fabrication steps: liftoff and dry etches fail if the resist layer is too thin.

Nevertheless, 100 nm features are consistently achievable with a 10 kV accelerating voltage through careful processing and patterning choices, even when bake temperatures must be kept low to avoid damage to sensitive materials. To demonstrate some important considerations, we fabricated sub-100 nm gap and line features using EBL followed by liftoff of 50 nm aluminum, varying several resist-related parameters between samples. Table 1 shows PMMA resist choices and bake times for four chips C1-C4. The resist labels of 495 or 950 describe the PMMA molecular weight in units of 10^3 g/mol. All resists chosen here are diluted in anisole; the notation AX in Table 1 indicates an X% anisole dilution. All bakes

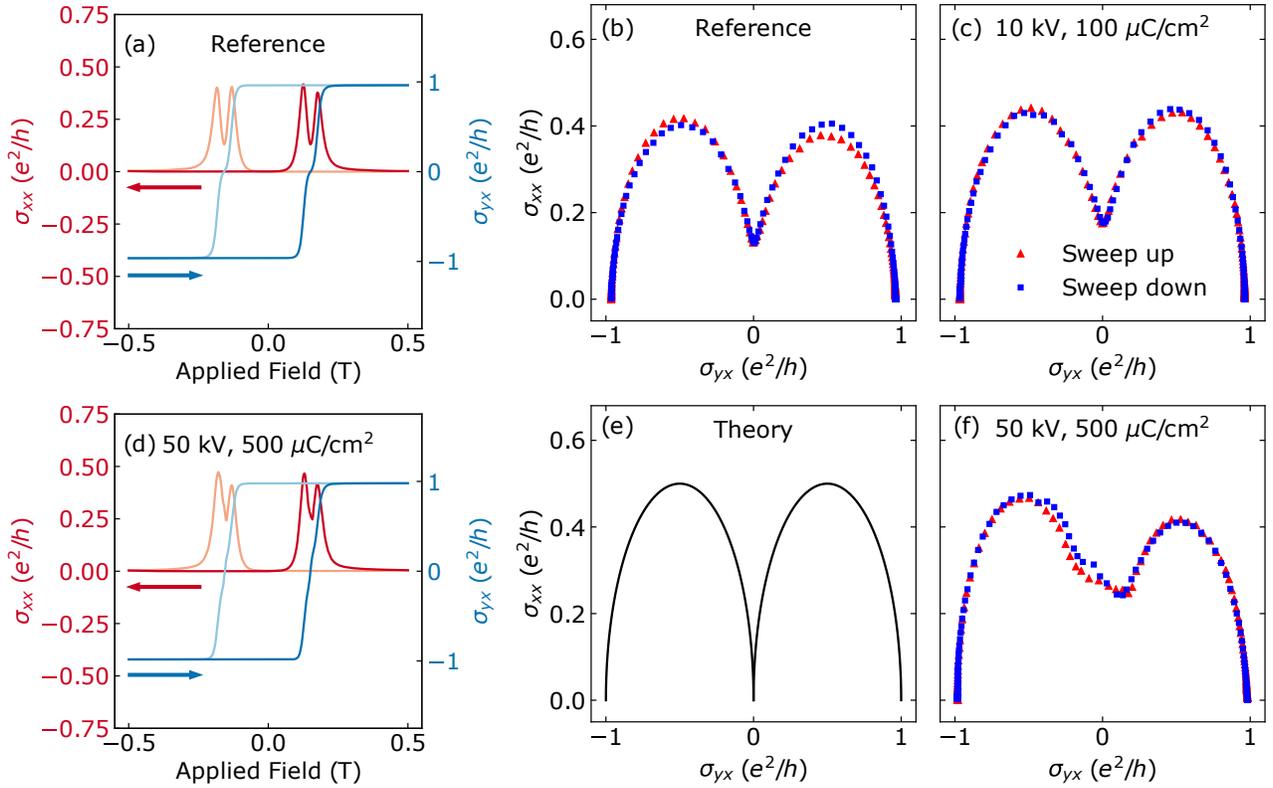


Fig. 3: Effects of electron beam exposure on electronic transport in Cr-BST. Longitudinal conductivity σ_{xx} (red, left axis) and Hall conductivity σ_{yx} (blue, right axis) are shown as a function of applied magnetic field for (a) a reference region, unexposed to an electron beam and (d) a region exposed at the clearing dose with a 50 kV accelerating voltage. Magnetic field was swept both up (darker traces) and down (lighter traces) to generate hysteresis loops. The same longitudinal conductivity data are plotted parametrically as a function of Hall conductivity for (b) the reference region and (f) the region exposed at the clearing dose at 50 kV. Additional parametric plots are shown for (c) the same measurement performed on a region exposed at the clearing dose with a 10 kV accelerating voltage and (e) theoretical behavior when the system is tuned explicitly through a trivial insulating phase upon magnetization reversal. In all parametric plots, data acquired while sweeping field up (down) are shown as red triangles (blue squares).

were performed in ambient atmosphere at a reduced temperature of 80° C to avoid thermal degradation of samples. The thinnest resist, used on C1 and C2, is approximately 130 nm thick, roughly as thin as possible for liftoff of 50 nm metal.

As discussed above, gaps were patterned by exposing two large areas separated by a nanometer-scale nominal gap size at varied doses. After development, a thin resist bridge (similar to Figure 4(c)) remained. Metal liftoff inverts the pattern, leaving behind two large metallized regions separated by a gap. This has long been a typical fabrication flow for liftoff-based weak link Josephson junctions [17, 47, 48]. Figure 5(a) shows representative results for

Table 1: Resist and bake time choices for four chips of Film 3 used to test EBL resolution with writes at 10 kV. All other processing parameters are described in the Methods section; notably, resist bake temperatures were limited to 80° C.

Sample	Resist (PMMA)	Bake Time (min.)
C1	950 A3	5
C2	950 A3	30
C3	950 A5	5
C4	495 A4/950 A3 bilayer	5/5

gaps fabricated on C1-C4; full results are shown in the supplemental materials.

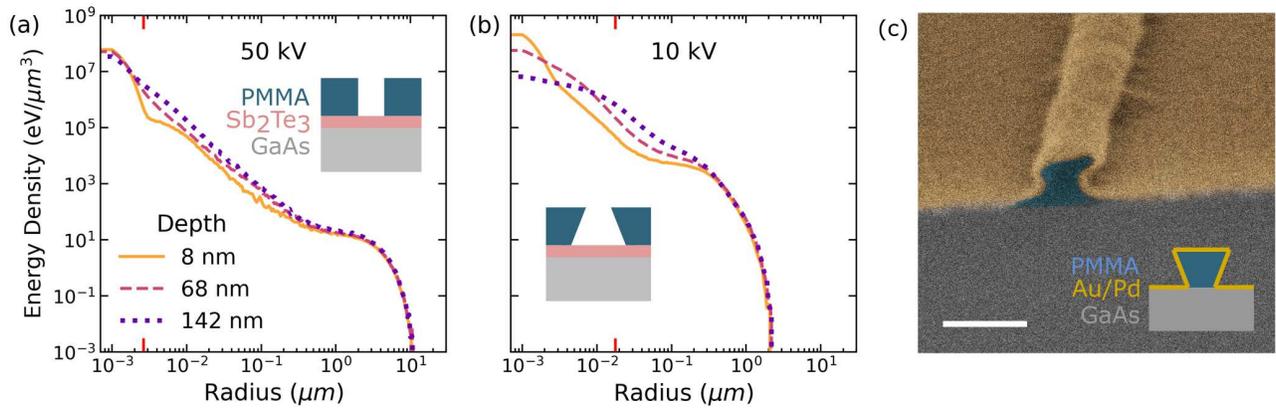


Fig. 4: (a,b) Simulated volumetric energy density deposited into a 150 nm layer of PMMA / 8 nm Sb₂Te₃ / 500 μm GaAs stack as a function of distance from the center of the electron beam. Data with an accelerating voltage of 50 kV [10 kV] are shown in (a)[(b)]. Line cuts are shown at three different depths from the top of the PMMA layers: 8 nm from the top (yellow line), 68 nm from the top (pink dashed line), and 142 nm (8 nm) from the top (bottom) of the resist layer (purple dotted line). Red markers on the axes indicate the radius at which deposited energy density decreases by an order of magnitude for the 142 nm traces, closest to the sample’s surface. Insets: expected cross-sectional profiles after exposure and development. Additional PSFs and discussion are presented in the supplemental materials. (c) False-color scanning electron micrograph of a cross-sectional profile of a thin resist bridge (center) after exposing the surrounding regions with a 10 kV electron beam and developing. Blue: PMMA. Gold: Au/Pd charge-neutralizing layer to aid in imaging. Grey: GaAs substrate. Scale bar: 100 nm.

Measured gap sizes down to 80 nm at best and 100 nm on average were attained. Chip 2, which featured a longer bake and thin resist, produced the best results overall and most consistently across different doses. C1, which featured a short bake and thin resist, also produced consistently good results, though slightly worse than C2. C3 and C4, with thicker resist stacks, produced worse results than C1 or C2, but still reached gaps less than 100 nm in some cases. Nominal gap sizes – the gap sizes of the pattern – were larger than measured gap sizes by roughly a factor of two, but the ratio varied between chips, doses, and the nominal gap sizes.

Thin lines were patterned by exposing a single pixel line (SPL) with the electron beam at various doses as discussed above. After development, metal deposition, and liftoff, a thin line of metal remains (Figure 5(b) inset). Such patterns are important for line gates or thin etched trenches [18, 19]. Figure 5(b) shows results for C1 and C2 with a 3 nm electron beam step size. Measured linewidth roughly increases with dose, as expected; past the clearing dose, features tend to broaden with increasing dose.

For both C1 and C2, lines down to about 100 nm wide were attained at the lowest successful line dose (C1: 1,300 pC/cm; C2: 1,200 pC/cm). Additionally, doses up to 50% larger produced consistent 100-120 nm lines. Additional results for a 5 and 8 nm step size are shown in Figure S9. Among the doses tested here, no viable lines were produced in Chips C3 and C4 because the thicker resists used on these chips require higher doses to fully expose deeper regions of the resist due to small-angle forward scattering.

The best results were obtained when using the thinnest resist layers, with 80-120 nm gaps and lines readily obtained within specific windows of dose and patterning parameters (nominal gap size, electron beam step size).

Thicker resist stacks produced some comparable gap sizes, but for a narrower range of processing parameters. The inferior performance of thicker resist at 10 kV accelerating voltage is consistent with the expectation of less mechanically-stable sidewalls and concomitantly increased sensitivity to patterning parameters. Comparing C1 and C2, increased bake times improved results. We speculate that longer

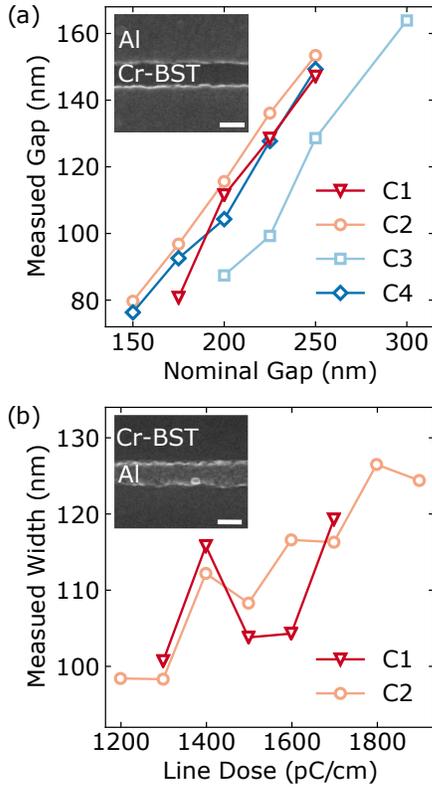


Fig. 5: Feature sizes for gaps and lines written with a 10 kV accelerating voltage. Insets: SEM images of smallest feature shown for C2; scale bar: 100 nm. (a) Measured gap width as a function of nominal gap width for C1-C4. Data were acquired for a range of doses; data shown here correspond to the dose at which the narrowest gaps were observed for each chip (C1: $110 \mu\text{C}/\text{cm}^2$. C2: $100 \mu\text{C}/\text{cm}^2$. C3: $130 \mu\text{C}/\text{cm}^2$. C4: $120 \mu\text{C}/\text{cm}^2$.). The full data set is presented in the supplemental materials. (b) Measured line widths as a function of line dose for chips C1 and C2 for single pixel lines written with a 3 nm step size. Data for 5 and 8 nm step sizes are shown in the supplemental materials.

bake times partially compensated for the low bake temperature used of 80°C , well below the $\sim 105^\circ \text{C}$ glass transition of PMMA.

CONCLUSIONS

In this paper, we demonstrated that electron beam lithography damages the topological insulator BST and its magnetic analogue Cr-BST. In the nonmagnetic material, we showed that exposure to electron beams increased electron density and decreased mo-

bility. In Cr-BST, we found that electron beam exposure altered the electronic transport of the material at the topological phase transition associated with magnetization reversal. Whereas here we measured degradation of bulk transport properties in regions uniformly exposed to electron beams, in real nanopatterned devices the electron dose received by the film varies spatially. In such devices, it becomes prohibitively challenging to separate fabrication-related materials damage from physics of interest.

Although we found that the severity of the changes to the materials' electronic properties after exposure at 30 and 50 kV accelerating voltages (at doses appropriate for lithography) are unacceptable for many experiments on TI nanostructures, we showed that lithography at 10 kV imparts minimal change to bulk electronic properties of canonical topological materials. Further study is required to elucidate the accelerating-voltage-dependent microscopic mechanisms of electron beam-induced damage, which may include creation of atomic point defects, or other structural materials changes.

Although increased small-angle scattering makes fine features difficult to pattern at 10 kV compared to at higher voltages, we demonstrated a window of processing parameters that generate 100 nm-wide lines or gaps after metal liftoff. Since 100 nm features are sufficient for many nanostructures of interest, we suggest that electron beam lithography at $\geq 30 \text{ kV}$ should be avoided in TI device fabrication. We further suggest that, when sub-100 nm features are required, electron beam lithography at intermediate accelerating voltages 15-25 kV could provide modest improvements in patterning resolution at the expense of small, but tolerable, increases in damage. Further work is required to quantify this trade-off. Additionally, alternative nanopatterning techniques have been developed, including selective area growth [49] and stencil lithography [28], although these techniques require specialized equipment, and materials damage (from, for example, unwanted interface chemistry) has not been explicitly studied.

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DATA AVAILABILITY STATEMENT

Point spread function simulations and transport data that support the findings of this study are available at <http://doi.org/10.5281/zenodo.7549123>. Scanning electron micrographs used to generate the data of Figure 5 are available from the corresponding author upon reasonable request.

AUTHOR DECLARATIONS

The authors have no conflicts to disclose.

AUTHOR CONTRIBUTIONS

Resources: L. P., P. Z., L. T., and K. L. W.; *Conceptualization:* M. P. A. and L. K. R.; *Methodology:* M. P. A., L. K. R., I. T. R., S. C. L., L. P., P. Z., L. T., and K. L. W.; *Investigation:* M. P. A. and L. K. R.; *Formal Analysis:* M. P. A. and L. K. R.; *Supervision:* M. A. K. and D. G.-G.; *Writing:* M. P. A. with input from all authors.

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Supplementary Materials

DETAILS OF EXPERIMENTAL METHODOLOGY

1.1 BST HALL BAR FABRICATION AND MEASUREMENTS

Two separate chips were cut from a single wafer of Film 1. On one chip, a Hall bar with three quartets of longitudinal and transverse contact pairs was fabricated as shown in Figure S1(a) to test the effects of 30 kV e-beam lithography. On the second chip, two Hall bars with structures identical to that shown in Figure S1(a) were fabricated and exposed to 10 kV electron beams (exposed regions with various fluences are shown in Figure S1(b,c)).

To define the sample mesa, Hall bars were patterned with photolithography (SPR 3612 resist, 2 min 80° C resist bake, phosphate salt developer followed by two water rinses) and etched in an Ar ion mill with an accelerating voltage of 300 V. Samples were cleaned with a 30 s acetone sonication and solvent rinse. Contacts were added with photolithography and electron beam (e-beam) evaporation of 5/80 nm Ti/Au after a 20 s *in situ* Ar pre-etch. Metal liftoff was performed with 20 s sonication in acetone and solvent rinse. The BST Hall bars were spin-coated with polymethyl methacrylate (PMMA) A5 950. Both chips were baked for 6 min at 80° C. At this point, isolated regions of the Hall bars were exposed to electron beams. All electron beam exposures on BST devices were performed on a FEI Nova NanoSEM. Writes at 10 kV used a 220 pA beam and 10 nm step size. Writes at 30 kV used a 600 pA beam and 10 nm step size. After exposure, the samples were developed for 50 s in a 1:3 solution of ambient-temperature methyl isobutyl ketone:isopropanol and photographed (Figure S1). The resist was then globally removed with a solvent rinse.

Electrical measurements of BST Hall bars were made in a variable temperature insert ⁴He refrigerator with a base temperature of ~1.55 K. A Stanford Research Systems SR830 lock-in amplifier (SR830) was used to source 5 V across a 1 GΩ resistor to provide a 5 nA RMS current bias at ~17 Hz. Measurements of longitudinal and Hall voltages as well as current were made by additional SR830s. Prior to measurement, voltages were amplified with using LI-75A voltage preamplifiers with a gain 10². Density and mobility values were extracted from Hall measurements as a function of applied out-of-plane magnetic field ranging from -0.5 T to +0.5 T. The Hall bar used for 30 kV accelerating voltage exposure was measured during a single cool-down. The two Hall bars used for 10 kV accelerating voltage exposure were measured during separate cool-downs.

1.2 CR-BST HALL BAR FABRICATION AND MEASUREMENTS

Hall bar mesas were patterned on the bare Cr-BST Film 2 with photolithography (SPR 3612 resist, 5 min 80° C resist bake, phosphate salt developer followed by two water rinses) and etched in an Ar ion mill with an accelerating voltage of 400 V. Samples were cleaned with a 20 s acetone sonication and solvent rinse. Contacts were added with photolithography and e-beam evaporation of 5/90 nm Ti/Au at a rate of 1 Å/s after a 10 s *in situ* Ar pre-etch. Metal liftoff was performed with a 20 s sonication in acetone and solvent rinse. The Cr-BST chip was spin-coated with polymethyl methacrylate (PMMA) A5 950 and baked for 5 min at 80° C. At this point, isolated regions of the Hall bars were exposed to electron beams. All electron beam exposures on Cr-BST devices were performed on a Raith VOYAGER electron beam lithography system. Writes at 10 kV used a 60 pA current and 5 nm beam step size. Writes at 50 kV used a 5 nA current and 10 nm beam step size. After exposure, devices were photographed (Figure S2) but not developed. Instead, the resist was globally removed with a solvent rinse. A seed layer of 1 nm aluminum was globally deposited with e-beam evaporation at 0.3 Å/s and allowed to oxidize in atmosphere. An alumina gate dielectric was then globally deposited with low-temperature (60° C) atomic layer deposition. Top gate electrodes were defined with photolithography, and e-beam evaporation was used to deposit 5/95 nm Ti/Au top gate electrode metals at a rate of 1 Å/s after 10 s *in situ* Ar pre-etch. Liftoff was performed with 20 s

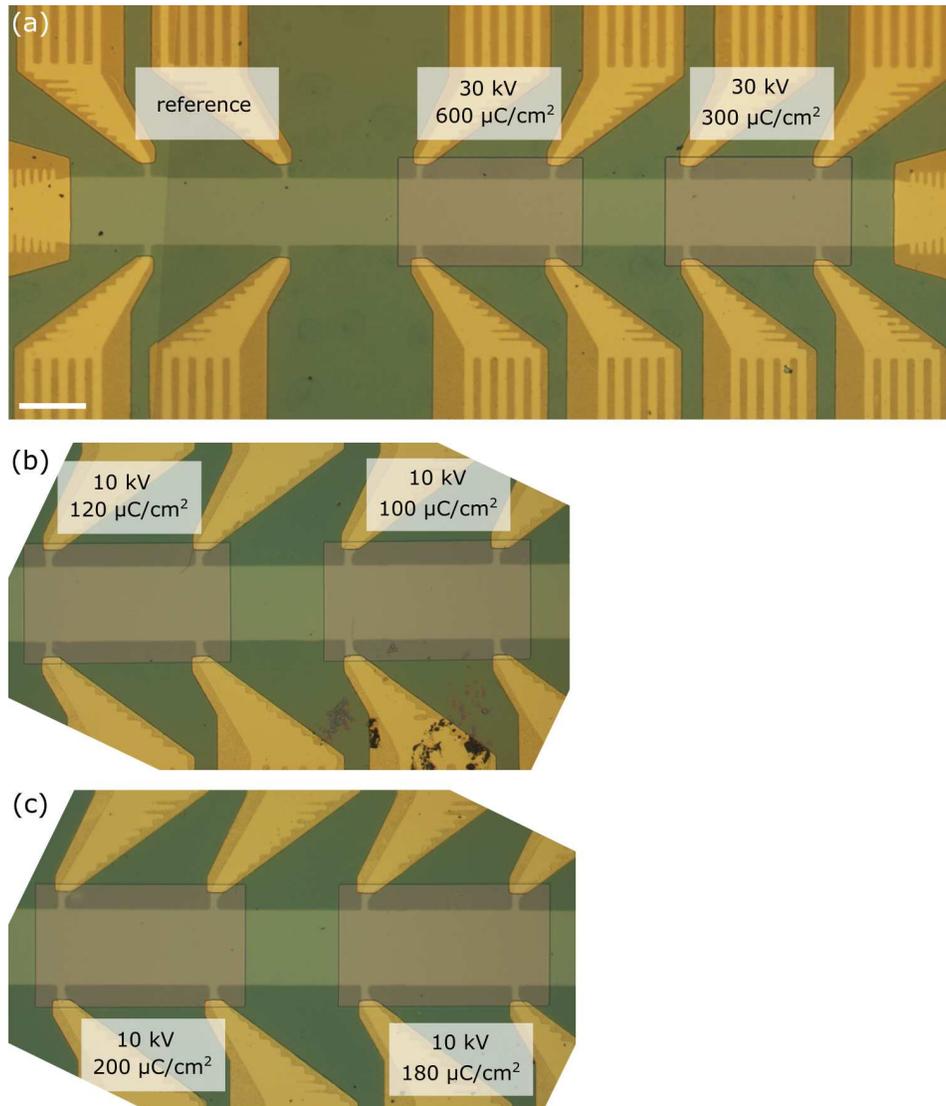


Fig. S1: Microscope images of Hall bar devices fabricated on BST and used to produce the data in Figure 2. Images were taken after electron beam exposure and development. (a) Long Hall bar with three quartets of contact pairs, with some regions (rectangles between middle and right contact pairs) exposed by a 30 kV electron beam and the indicated doses. Picture shown was stitched together from two separate images (break between images falls in the reference region). Scale bar: $80\ \mu\text{m}$. (b,c) Regions of two separate Hall bars exposed to a 10 kV electron beam at the indicated doses. Only the exposed regions are shown, but the full device geometries are identical to that shown in (a). Both images are irregular shapes because the original images were taken at an angle, and then cropped to show the regions of interest.

acetone sonication and solvent rinse. Excess dielectric was removed over the Hall bar mesa contacts with a photolithographically-masked tetramethylammonium hydroxide-based wet etch (120 s/20 s/20 s Microposit CD-26 Developer/water/water). The resist was then globally removed with a solvent rinse.

Electrical measurements of Cr-BST Hall bars were made in a dilution refrigerator with a base temperature of $\sim 30\ \text{mK}$ after magnetizing the sample with a 0.5 T out-of-plane applied field. The measurement lines include low-pass RF filters as well as discrete RC filters at the mixing chamber stage. A Stanford Research 830 lock-in amplifier (SR830) was used to source 5 V across a $1\ \text{G}\Omega$ resistor to provide a 5 nA current bias at $\sim 5\ \text{Hz}$. Measurements of longitudinal and Hall voltages as well as current were measured by additional SR830s as well as Stanford Research 860 lockin amplifiers. Prior to measurement, voltages were amplified

with either separate NF LI-75A voltage preamplifiers or a single NF multi-channel preamplifier, with a gain of 10^2 V/V in either case. Current was amplified with an Ithaco 1211 current preamplifier with a gain of -10^6 V/A. Gate voltage was controlled with a Keithley Model 2400 Source-Measure Unit. Temperature was modulated with a heater on the mixing chamber stage of the dilution refrigerator, and was measured by a thermometer also on the mixing chamber stage. Each Hall bar on the Cr-BST chip was measured on a separate cool-down.

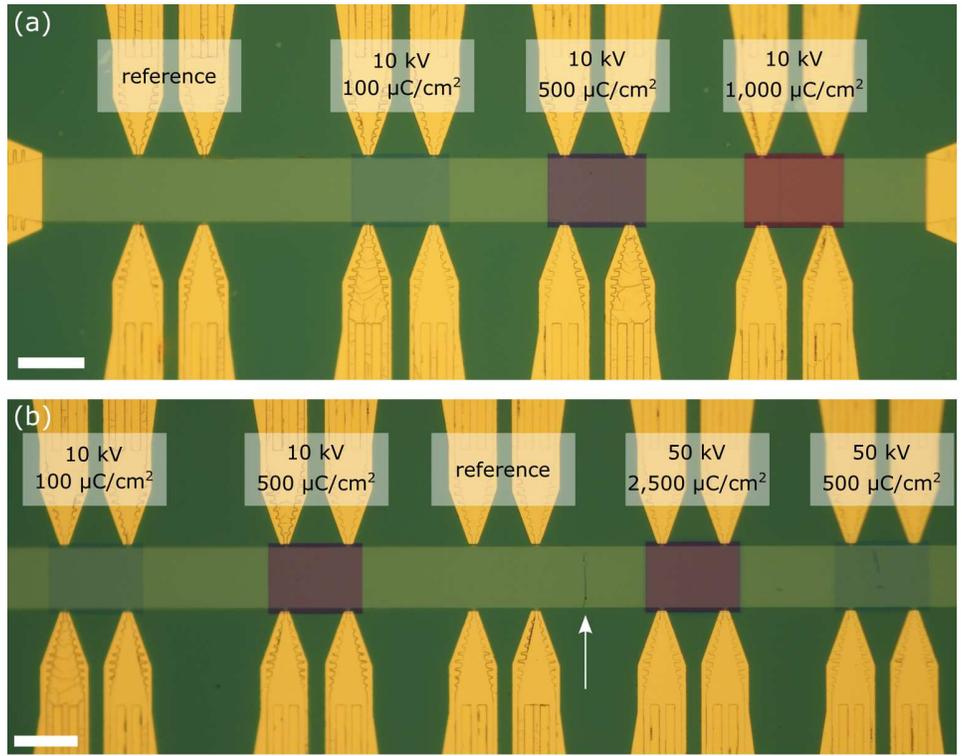


Fig. S2: Microscope images of Hall bar devices fabricated on Cr-BST and measured to produce Figure 3. Devices are shown after electron beam exposure, with undeveloped resist still in place. Exposed resist is visible as the colored squares over individual sets of contacts. These images are not false-colored; the exposed resist has colors different from unexposed resist. Exposure conditions are indicated for each exposed region. Scale bars, $80 \mu\text{m}$. (a) Hall bar exposed exclusively at 10 kV and used for measurements in Figure 3(a-c). (b) Hall bar exposed at both 10 and 50 kV and used for measurements in Figure 3(d,f). The Hall bar mesa was damaged between the reference and 50 kV regions (indicated by arrow), but this damage had no noticeable impact on measurements in the QAHE regime.

ADDITIONAL BST DAMAGE DATA

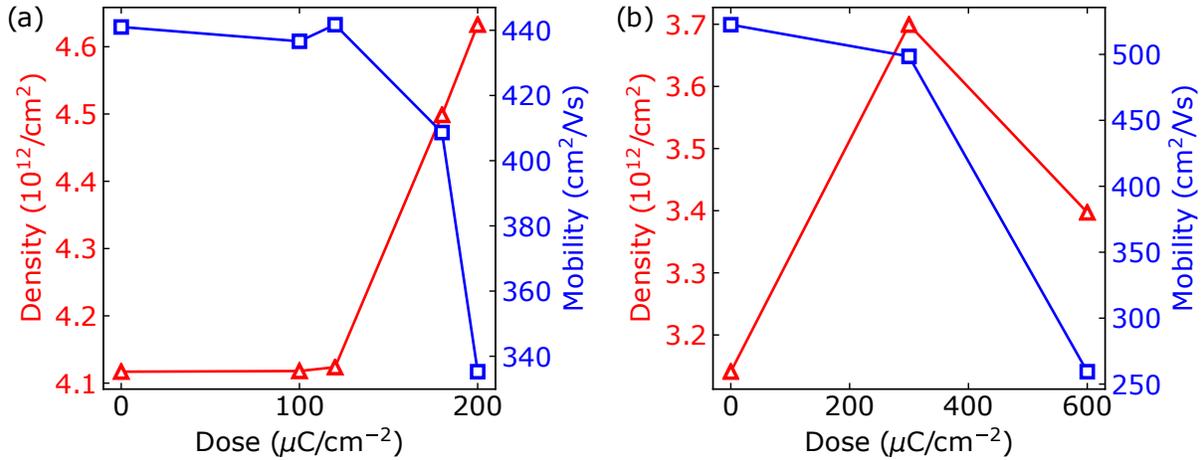


Fig. S3: Raw data used to generate Figure 2. Density (red triangles, left axis) and mobility (blue squares, right axis) as a function of dose for regions of a BST Hall bar exposed at (a) 10 kV or (b) 50 kV.

ADDITIONAL CR-BST DAMAGE DATA

A temperature scale T_0 corresponding to an effective size of the magnetic exchange gap can be extracted from longitudinal and Hall transport measurements at elevated temperatures. As temperature is increased, some fraction of charge carriers are thermally excited across the magnetic exchange gap into surface state bands; these thermally activated carriers introduce dissipation into an otherwise dissipation-free system. Arrhenius fits of longitudinal conductivity can provide T_0 as the barrier to thermally activated dissipative conduction. At lowest temperatures, measurements typically plateau and diverge from a simple Arrhenius model due to deviation of electron temperature from lattice temperature and leakage currents in measurement electronics; as a result, an Arrhenius plus offset model ($\sigma_{xx} = a + b \exp -T_0/T$ with free parameters a and b) is often used to fit T_0 .

Fit values for T_0 are maximal when the Fermi level sits in the middle of the magnetic exchange gap: if the Fermi level is offset from the middle of the gap, the barrier to thermal excitation across the gap, and therefore the fit value of T_0 , is reduced. Figure S4(a,b) plots the temperature scale for thermally activated conduction for Hall bar regions exposed to electron beams under various conditions as a function of electrostatic gate voltage (V_g). The electrostatic gate voltage for which T_0 is maximal corresponds to the Fermi level sitting in the middle of the gap; this gate voltage is called the optimal gate voltage, V_{opt} .

Shifts in optimal gate voltage between samples indicates a shift in the native Fermi level, caused by doping. Figure S4(c) shows shifts in V_{opt} as a function of dose factor for exposures at 10 and 50 kV. All data points are compared to the optimal gate voltage in the reference regions, $V_{opt,0}$. For the 10 kV region exposed at the clearing dose, $V_{opt} - V_{opt,0} < -0.2$ V. Comparing decreases in T_0 to the magnitude of gate voltage excursions, -0.2 V is considered a negligible shift in V_{opt} . This minimal shift in V_{opt} , which increases linearly with dose factor, indicates a systematic doping of the Cr-BST material with 10 kV electron beam exposure. For regions exposed at 50 kV, however, $V_{opt} - V_{opt,0}$ is a more substantial -0.6 V for the exposure at the clearing dose. Additionally, V_{opt} does not shift monotonically with dose.

Figure S5 shows measurements of longitudinal and Hall conductivity acquired as a function of applied magnetic field for all of the Cr-BST Hall bar regions shown in Figure S2(a) as well as the regions exposed at 50 kV shown in Figure S2(b). A subset of this dataset is shown in Figure 3. Regions of the Hall bar shown in Figure S2(b) that duplicate regions shown in Figure S2(a) produced quantitatively similar measurements to their counterparts.

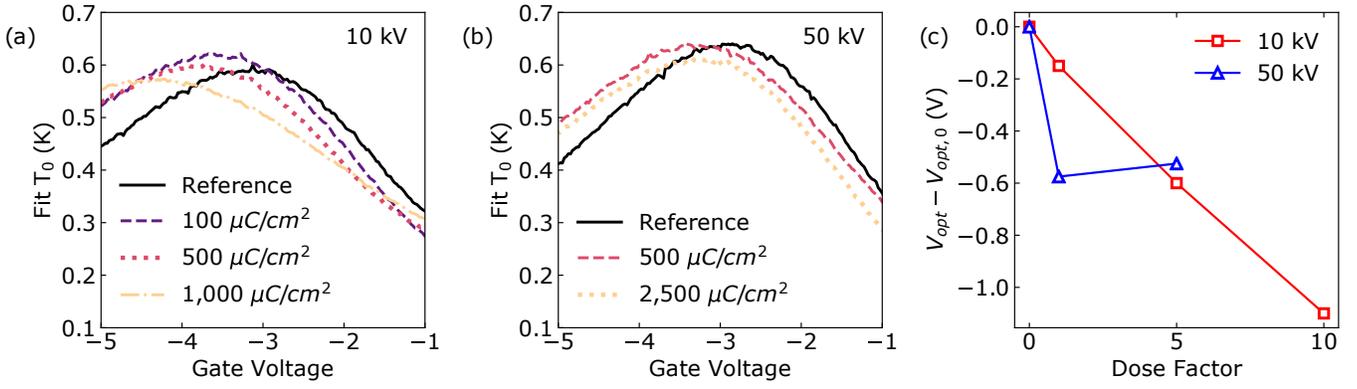


Fig. S4: Temperature scales extracted from an Arrhenius plus offset model as a function of gate voltage for regions of Cr-BST Hall bars exposed at (a) 10 kV and (b) 50 kV. Maxima are taken as the effective size of the magnetic exchange gap, and the corresponding gate voltage as tuning the Fermi level to the center of the gap. (c) Shifts in optimal gate voltage compared to reference regions for exposures at 10 kV (red squares) and 50 kV (blue triangles). Data is plotted as a function of dose factor relative to the clearing dose; at 10 (50) kV, the clearing dose is 100 (500) $\mu\text{C}/\text{cm}^2$.

Regions exposed at 10 kV deviate monotonically from the behavior shown in the reference region. All data shown in Figure S5 were taken at or near V_{opt} for each region, which rules out Fermi level shifts as the cause of this variation. Rather, it appears that behavior across the topological phase transition changes with dose after 10 kV exposures. In the reference region and the region exposed at the 100 $\mu\text{C}/\text{cm}^2$ clearing dose, the system tunes somewhat explicitly through a trivial insulating $C = 0$ phase at magnetization reversal as discussed in the main text. As dose is increased, the system appears to tend towards a direct $C = -1 \leftrightarrow C = +1$ transition.

Regions exposed at 50 kV, however, demonstrate different behavior. A repeatable, non-hysteretic asymmetry in behavior across magnetization reversal is apparent even at the 500 $\mu\text{C}/\text{cm}^2$ dose. While we currently lack an explanation for this dramatic change in phenomenology, we posit it may indicate higher damage at one surface of the Cr-BST thin film than the other. Since the film under study is a modulation-doped film with an enhanced Cr concentration at the top and bottom surface, selective damage to one surface over the other may introduce some asymmetry upon reversing magnetization.

The differences in behavior between regions exposed at 10 versus 50 kV suggest an accelerating-voltage-dependent damage mechanism even when controlling for dose; comparing regions exposed with a 500 $\mu\text{C}/\text{cm}^2$ dose, the region exposed at 10 kV performs more similarly to the reference region than the region exposed at 50 kV.

ADDITIONAL TEST LITHOGRAPHY DATA

Figure S6 shows point spread functions calculated in the same manner as those shown in Figure 4(a,b) for a range of accelerating voltages 5-100 kV. From 100 kV down to 25-30 kV, the bulk of the energy density is deposited within 10 nm of the beam center. For lower accelerating voltages, small-angle forward scattering becomes more significant and the energy density spreads laterally as electrons progress down into the resist stack. The low plateaus in energy density at radii far from the beam center are caused by electrons that backscatter off of the Sb_2Te_3 surface and return upwards through the resist.

The risk associated with small-angle scattering of electrons through thicker resists is demonstrated in Figure S7, which shows a thin resist bridge that completely delaminated from the substrate after patterning at 10 kV and development. In this case, A5 950 PMMA was spin-coated onto a bare GaAs substrate and baked for 5 minutes at 80° C. The resist was exposed with a 100 $\mu\text{C}/\text{cm}^2$ dose and a 10 kV accelerating voltage on

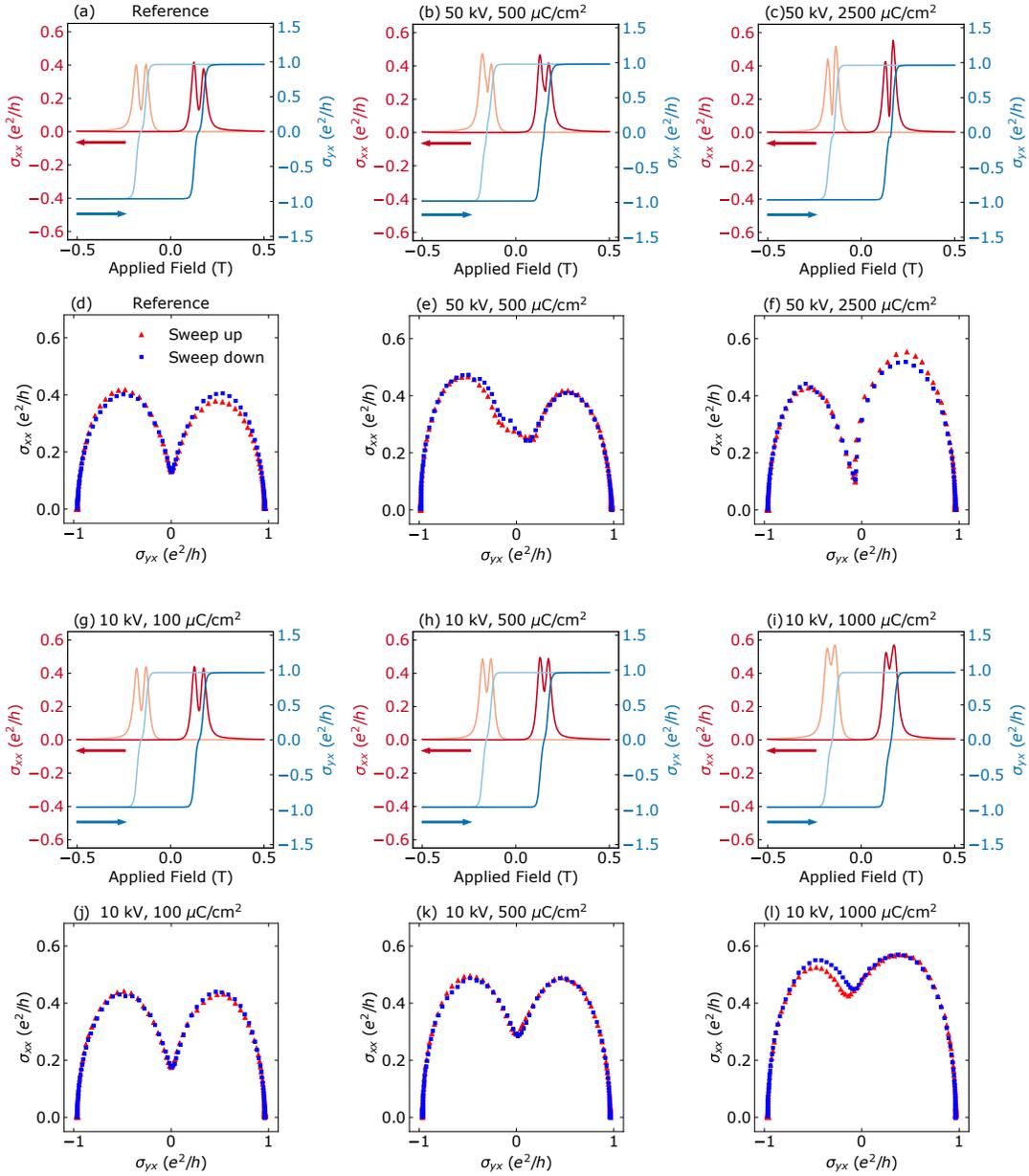


Fig. S5: Extended dataset for electronic transport measurements of Cr-BST Hall bars across magnetization reversal. Vertical pairs of subplots correspond to measurements of a specific localized region that was exposed with an electron beam as denoted in the subplot title. Data in subplots (a, b, d, f, g) are reprinted from Figure 3. (a-c,g-i) Longitudinal and Hall conductivities as a function of applied magnetic field. Longitudinal conductivity is shown in red and plotted on the left axis, while Hall conductivity is shown in blue and plotted on the right axis (axis indicated by arrows). Data taken while sweeping field from negative to positive (positive to negative) is shown in darker (lighter) colors. (d-f,j-l) Parametric plots of longitudinal conductivity as a function of Hall conductivity as magnetic field is increased (red triangles) or decreased (blue squares). All data was taken at or near the optimal gate voltage for each pair: (a,d) $V_g = -3$ V. (b,c,e,f) $V_g = -3.2$ V. (g,h,j,k) $V_g = -3.8$ V. (i,l) $V_g = -4.2$ V.

a Raith VOYAGER electron beam lithography system and developed for 55/20 s 1:3 MIBK:IPA/IPA. A 4 nm 60/40 Au/Pd charge-neutralizing layer was added before imaging.

As described in the main text and shown in Figure 5(a), EBL writes with a 10 kV accelerating voltage

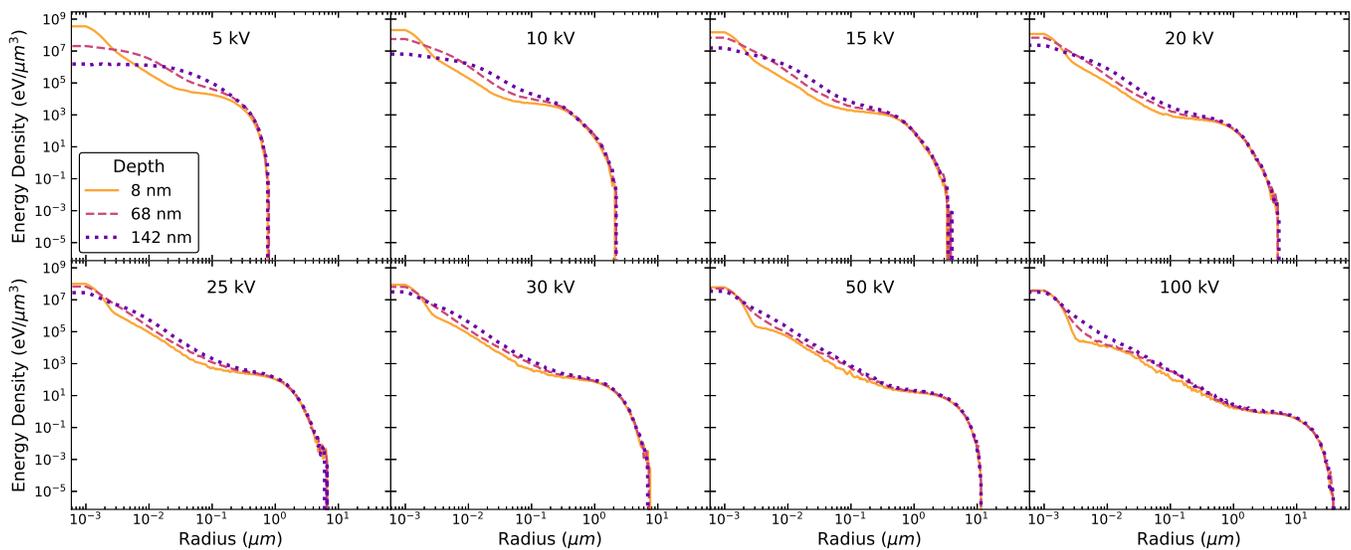


Fig. S6: Simulated point spread functions for an electron beam exposure on a 150 nm PMMA / 8 nm Sb_2Te_3 / 0.5 mm GaAs stack for accelerating voltages 5-100 kV. Each subplot shows linecuts of energy density as a function of radius from the center of the electron beam point source at several depths into the PMMA in the same format as Figure 4(a,b). Linecuts at 8 nm, close to the top of the PMMA, are shown as yellow solid lines. Linecuts at 68 nm, towards the middle of the PMMA, are shown as pink dashed lines. Linecuts at 142 nm, close to the surface of the substrate, are shown as purple dotted lines.

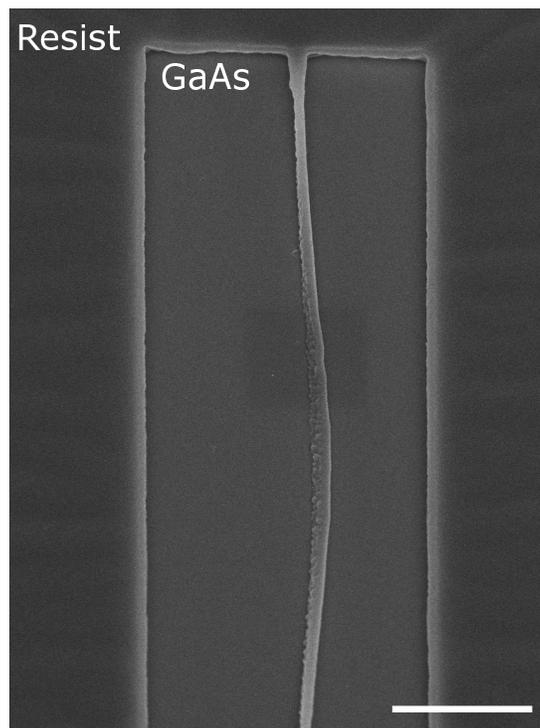


Fig. S7: SEM image of developed resist after exposure with a 10 kV electron beam. Because the resist was too thick, the thin resist bridge was completely undercut and delaminated from the substrate. The slightly darker square in the middle of the image is a result of carbon contamination deposited during acquisition of a different SEM image. Scale bar: $1\mu\text{m}$

were used to produce thin gaps of BST after resist development, metallization, and liftoff. The complete dataset, including all e-beam doses and nominal gap sizes for all four chips C1-C4, is shown in Figure S8. For all four chips, measured gaps below 100 nm in width were attained for some set of patterning parameters.

Nominal gap sizes are necessarily larger than the measured gap sizes due to broadening of the pattern during the write. Where nominal gap sizes become too small, typically < 150 nm, the thin resist bridge left behind after development can become completely undercut and delaminate entirely (Figure S7). For chips C1 and C2, nominal gap size nearly linearly tunes the measured gap size below 150 nm. For C3 and C4, measured gaps changes monotonically but not quite linearly with nominal gap size.

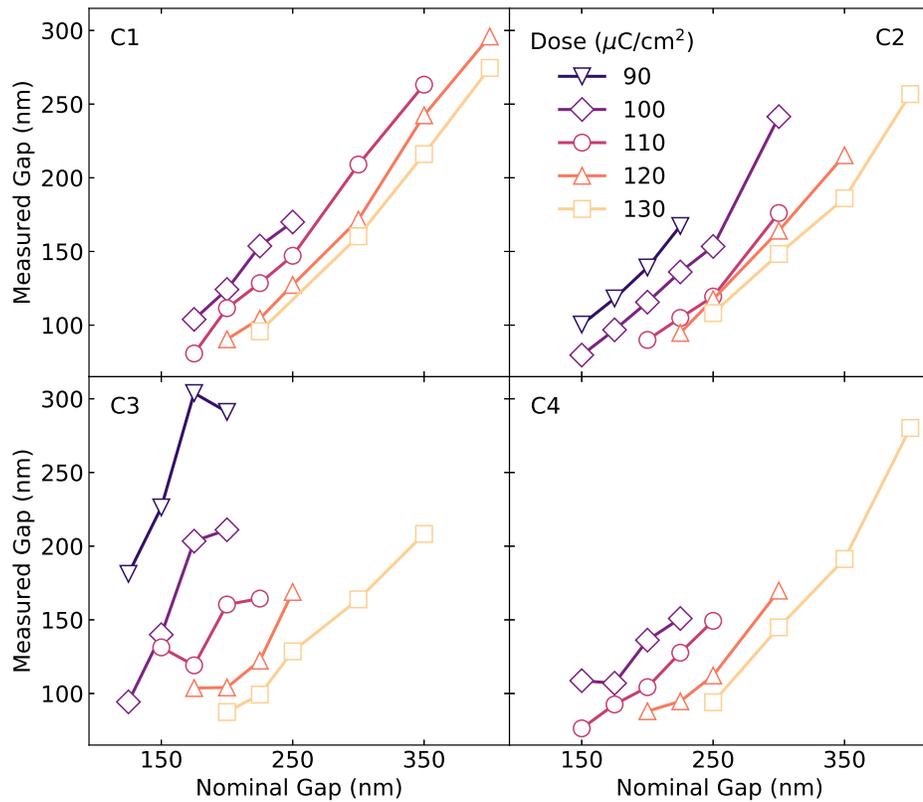


Fig. S8: Full data for size of thin gaps patterned at 10 kV on C1-C4; processing details are described in the main text. Each subplot shows measured gap size after metallization and liftoff plotted against the nominal written gap size. Individual lines represent exposures at a specific dose. Where specific doses or nominal gap sizes are omitted, either liftoff failed and metal shorted across the gap or gaps were quite large. Data shown in Figure 5(a) comes from the dose that produced the smallest gaps.

Complete datasets for thin lines patterned with a 10 kV accelerating voltage are shown in Figure S9 for C1 and C2. In addition to single pixel lines written with a 3 nm beam step size (as described in the main text and shown in Figure 5(b)), SPLs were also written with 5 and 8 nm step sizes. For all three step sizes, lines thinner than 120 nm were consistently produced across a wide range of doses.

On C1, linewidths remain consistently 100-120 nm across all measured doses. On C2, in contrast, dose roughly monotonically tunes the measured linewidth between ~ 90 -140 nm over the same dose range.

