

Modular decoding: parallelizable real-time decoding for quantum computers

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Universal fault-tolerant quantum computation will require real-time decoding algorithms capable of quickly extracting logical outcomes from the stream of data generated by noisy quantum hardware. We propose *modular decoding*, an approach capable of addressing this challenge with minimal additional communication and without sacrificing decoding accuracy. We introduce the *edge-vertex* decomposition, a concrete instance of modular decoding for lattice-surgery style fault-tolerant blocks which is remarkably effective. This decomposition of the global decoding problem into sub-tasks mirrors the logical-block-network structure of a fault-tolerant quantum circuit. We identify the *buffering condition* as a key requirement controlling decoder quality; it demands a sufficiently large separation (buffer) between a correction committed by a decoding sub-task and the data unavailable to it. We prove that the *fault distance* of the protocol is preserved if the buffering condition is satisfied. Finally, we implement edge-vertex modular decoding and apply it on a variety of quantum circuits, including the Clifford component of the 15-to-1 magic-state distillation protocol. Monte Carlo simulations on a range of buffer sizes provide quantitative evidence that buffers are both necessary and sufficient to guarantee decoder accuracy. Our results show that modular decoding meets all the practical requirements necessary to support real-world fault-tolerant quantum computers.

I. OVERVIEW OF RESULTS

In this article, we present and analyze **modular decoding**, a general method for decomposing decoding problems into smaller decoding sub-tasks. This decomposition allows meeting the practical requirements of a fault-tolerant quantum computer. Firstly, modular decoding allows concurrent execution by construction, which allows side-stepping throughput limitations associated to any single processing core executing the decoding algorithm. More importantly, modular decoding is a real-time (live) approach to decoding, providing intermediate logical outcomes with minimal latency. This is an essential, yet often overlooked, requirement to enable universal fault-tolerant quantum computation.

We identify **buffering** as the key technique enabling modular decoding to produce high quality decoding results. The *buffering condition* requires the input to each decoding task to include a *buffer* of additional outcome data in directions where previous decoding tasks have not set fixed boundary condition. The buffer for each decoding task can be determined by a graph algorithm which works for arbitrary modular decoding decompositions.

We prove a rigorous **soundness theorem for modular decoding**, which guarantees that decoding on a modular decomposition can be as effective at catching errors as an *offline decoder* accessing the entire decoding problem. The only assumptions are that each decoding sub-task is solved using a sound decoder, and provided a sufficiently large buffer of outcome data (termed the *buffering condition*).

We introduce **edge-vertex decoding**, a concrete instance of *modular decoding* well suited to lattice-surgery style fault tolerance. This approach follows the quantum circuit structure distinguishing two kinds of decoding sub-tasks. Each corresponds to either an elementary logical block (*vertex task*) or

to a connection among neighboring elementary blocks (*edge task*). All edge decoding tasks can be solved in parallel and only require a buffer of outcome data. Vertex decoding tasks require boundary condition data from neighboring edge tasks but can otherwise be solved independently and in parallel. By design, the use of buffers guarantees maintaining decoding quality (soundness), whereas the minimal size of decoding sub-tasks and their data dependencies reduces logical outcome latency.

We **implement** edge-vertex decoding decompositions and **numerically benchmark** the decoding quality against offline decoding via Monte Carlo simulations. We find evidence that a buffer width commensurate with the protocol distance is both necessary and sufficient to maintain the same decoding performance as offline decoding. Our numerical simulations, which include large-scale **15 to 1 magic state distillation**, access logical block networks significantly more complex than current literature.

A. Outline and readers guide

The article is organized as follows. **Sec. II** provides general background on quantum computing, fault-tolerance and decoding. It also motivates the need for modular decoding using unitary gate synthesis as an example, and present connections with previous work. It can be safely skipped by an expert reader who wishes to go directly to more technical material. **Sec. III** establishes technical notation and concepts relevant to decoding which will allow precise formulation of algorithms and theorems in later sections. In **Sec. IV**, we introduce the modular decoding problem, which involves decomposing the global problem into smaller, decoding sub-tasks such that their results can be straightforwardly combined into a global correction. We show naive modular decoding effectively decreases the fault distance, and show how buffering can be used to overcome this. **Sec. V**, we prove that buffer-

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ing is sufficient to maintain decoder soundness—that errors with weight up to half the fault distance can still be corrected, given a sufficient buffer. The proof may be skipped by readers who are not mathematically inclined. **Sec. VI** we introduce methods to schedule the various modular decoding sub-tasks, and introduce the edge-vertex decoder which has very low reaction time. **Sec. VII** presents extensive simulation data for edge-vertex modular decoding, including complex logical block networks in the fault-tolerant 15-to-1 magic-state distillation protocol. We conclude in **Sec. VIII**, which summarizes our work and discusses directions for further research.

II. BACKGROUND AND MOTIVATION

Universal quantum computers can efficiently solve problems which are otherwise intractable for their classical counterparts. Noise, imperfections and errors have thus far hindered scaling up from the realm of intermediate scale quantum devices (NISQ) [1] to a regime of useful large scale quantum computers. Fault tolerance (FT) prescribes how to overcome this; scale up the number of quantum components while maintaining individual error rates per physical operation *below threshold*.

Quantum computers seek to answer otherwise inaccessible computational problems. In fault-tolerant quantum computing, these answers are encoded in physical measurement outcomes and can only be reliably extracted by compensating for the diagnosed noise. Thus the *logical outcome* information needs to be *decoded* from vast amounts of classical data. The *decoder subsystem* is responsible for this task and may be implemented by any combination of software, firmware or hardware adequately processing the classical data.

A decoder is good if it produces reliable logical outcomes. This allows comparing decoders operating under the same fault-tolerant protocol and physical error model. A better decoder will boast consistently lower *logical error rates* (LER).

Modeling the decoder as a monolithic function or algorithm implicitly assumes that all physical measurement data can simultaneously be made available as the decoder’s input. This situation is often referred to as *offline decoding*, as it is compatible with storing all the *physical* outcome data produced during of a fault-tolerant quantum computation and decoding *logical* outcomes from it at a later time (i.e., offline). Most academic literature assumes this offline decoding idealization; this simplifies decoder implementation and allows comparing LER and threshold performance among decoders.

However, decoded outcomes need to become available throughout the computation. The decoding process must quickly provide partial results on the logical outcomes in terms of available physical outcomes. In general, the entirety of the quantum circuit is not even defined as subsequent quantum gates may be chosen depending on logical outcomes obtained. This means that, in practice, decoding can not be modeled as a monolithic offline process but rather *online* as a *streaming* transformation of physical outcomes into logical outcomes.

The time taken from the moment relevant physical mea-

surement outcomes become available to the time the decoded logical outcomes can be used to control further logic is called the *reaction time*. The reaction time should be kept short, as it can potentially limit the rate of logic gates (such as T -gates), as illustrated by the example of arbitrary angle rotations (see Fig. 1). Contributions to the reaction time come from the classical processing time required for (partial) decoding as well as communication latency.

If the decoder can not keep up with the outcome data rate (also called throughput), the quantum computation may be forced to idle (i.e., perform identity gates) until a conditional follow-up operation can be determined, and in the process generate more syndrome data to be processed. This approach leads to a *decoding back-log* [2, 3] growing exponentially with the depth of the logical adaptivity and the *reaction-time* growing exponentially as the quantum circuit progresses. Thus, the decoders processing throughput must fully cover the outcome data throughput to keep the reaction-time constant (and hopefully small).

Which outcomes are considered relevant for decoding a logical outcome is a critical choice which impacts both the reaction time and logical error rate. Our main contribution is to provide a *modular decoding algorithm*, wherein sensible choices for relevant inputs can lead to logical error rates which are close to optimal and a uniform reaction time which is independent of the quantum algorithm being executed.

The overall decoder *throughput* (i.e. the speed at which data is processed) can be increased by decomposing the global decoding problem into independent *decoding sub-tasks* and distributing these among multiple *decoder units* which operate in parallel. However, the decoding tasks can not be made fully independent of each other, as their joint outcomes must be consistent with the observed syndrome. In this article, we show that it is possible to minimize the data dependency among these decoding tasks in such a way that a reaction-time independent of the quantum circuit size can be achieved. The joint throughput of the decoder units only needs to exceed the production rate of physical outcome data by a constant factor as some outcome data may be processed by multiple decoder units.

A. Motivating example: intermediate logical outcomes in gate synthesis

To motivate the need for low-latency decoders (i.e., low reaction time), we consider the problem of *gate synthesis* in surface code fault-tolerance. This refers to approximating arbitrary single-qubit gates as products of T gates ($\pi/8$ -rotations in the Z basis) and Clifford operations. This decomposition is representative and of widespread practical relevance. As we will see, a natural implementation of this sub-routine involves adaptive sequences of operations wherein each operation is conditioned on a logical measurement outcome from the immediately preceding one. This motivates the need for a decoding approach which can provide logical measurement outcomes as soon as possible.

The Matsumoto and Amano normal form [4, 5] is presented

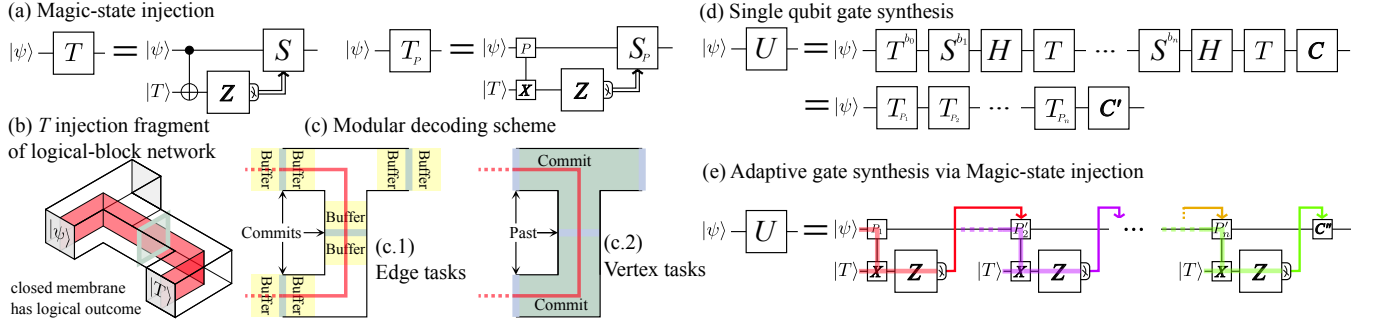


FIG. 1. **(a) (left)** A T gate is applied via magic state injection and requires a Clifford correction S conditioned on the Z measurement outcome on the second qubit. This measurement outcome requires the Pauli frame for $Z \otimes Z$ on the inputs. **(a) (right)** The protocol can be generalized to realize a generalized T gate $T_P := \exp(i\pi/8P)$ by applying a generalized CNOT. **(b)** An isometric view of a 3D logical-block network fragment corresponding to magic state injection of (a) for a $T = T_Z$ gate. The outcome dependent S gate correction is not included as it can be efficiently tracked classically. The logical membrane highlighted in red closes to produce a logical outcome (the Z measurement outcome of a). The interface between two logical-blocks is highlighted in green. Both membrane and interface are bookkeeping tools, neither having a physical signature. **(c)** A 2D top-view schematic for the edge-vertex modular decoding decomposition for the fragment of logical-block network presented in (b). The *edge-vertex* modular decoding decomposition first solves edge decoding tasks (c.1) using syndrome data from in neighbouring buffer regions (yellow). After edge decoding tasks are complete, vertex decoding tasks (c.2) can be solved independently, each task having boundary conditions set by neighbouring edge tasks. This scheme has very fast reaction times, as there is no significant chain of dependencies between decoding tasks. **(d)** In gate synthesis, arbitrary single qubit unitaries may be approximated by a sequence of T gates interspersed with $\{SH, H\}$ Clifford gates and a final Clifford gate C or alternatively as a sequence of generalized T gates. **(e)** When T gates are performed via magic state injection, each logical outcome b_j obtained during injection may require an additional S_j correction. These logical outcomes correspond to partially highlighted logical membranes represented in more detail in (b) or (c). Each of these membranes continue and branch into the past but can be efficiently summarized by the logical Pauli frame which tracks their cumulative value. As an alternative to physically implementing S corrections, these may be incorporated in a Clifford frame, modifying which generalized T gate is to be performed next. Specifically, each P'_k is given by $P'_k := C_k P_k C_k^\dagger$, with $C_k := S_{P_1}^{b_1} \dots S_{P_{k-1}}^{b_{k-1}}$. Similarly $C'' := C_n C' C_n^\dagger$, which need not be physically implemented. Colored arrows illustrate when and where the logical outcomes b_j are needed to condition further logical blocks.

in the first line of Fig. 1 (d) and can be used to express arbitrary products of Clifford and T gates in a way that minimizes the number of T gates. An operator HS^{b_j} , with $b_j \in \{0, 1\}$ is applied between otherwise consecutive T gates. In particular, efficient (in number of T gates) approximations of single qubit unitaries such as those used for gate synthesis can be presented in this form. Selinger and Ross provide an efficient algorithm to find the exponents b_j best approximating rotations around the Z axis [6].

As an alternative to the Matsumoto and Amano form, the intermediate Clifford operators can be avoided by appropriately conjugating each of the T gates involved in the sequence. This results in a sequence of n generalized T gates $T_P := \exp(i\pi/8P)$, followed by a single Clifford operator C' as shown in the second line of Fig. 1 (d). Valid sequences $C' T_{P_n} \dots T_{P_2} T_{P_1}$ are characterized by two conditions: i) $P_i \in \{X, Y, Z\}$ (i.e., no minus signs on Paulis) and ii) consecutive gates $T_{P_i}, T_{P_{i+1}}$ are distinct ($P_i \neq P_{i+1}$).

Neither T gates nor generalized T_P gates can be achieved exclusively with lattice surgery. However, each T -gate can be realized by injecting a distilled magic-state $|T\rangle$, as shown in Fig. 1 (a)(left), whereby a measurement is performed which teleports the T gate into the data qubit up to a conditional S gate correction. A generalized T_P gate (instead of $T \equiv T_Z$) can also be realized in a similar manner as shown in Fig. 1 (a)(right). To do so, the CNOT and S unitary operations in the injection protocol must be replaced by Clifford C conjugated versions (where C acts on the first qubit such that

$P = CZC^\dagger$). In other words, instead of a CNOT operator, a generalized C_P NOT = $(II + PI + IX - PX)/2$ is applied and the correction $S_P := \exp(i\pi/4P)$ (instead of S) is required conditional on the measurement outcome.

If generalized T_P gates are performed via magic state injection, then each one will involve the measurement of a logical outcome and the application of a S_P correction conditioned on the outcome of said measurement. Logical outcomes will also be needed immediately if S_P corrections are tracked as a Clifford frame (i.e. conjugate all forthcoming operations) rather than performing them explicitly. This is illustrated in Fig. 1(e), where each logical outcome condition the choice of the next generalized T_P gate. The auto-corrected $\pi/8$ gates introduced in [7] are a resource efficient alternative which reaps the most benefit from the short reaction times which can be achieved via modular decoding.

For concreteness, we illustrate fault-tolerant quantum computations using *surface codes* and *lattice surgery* [7, 8], where quantum algorithms are represented by 3D space-time networks of logical blocks [9], each element of which is a 3D block representing a FT quantum instrument. Such blocks have input/output ports which can be composed across to represent quantum circuit topology.

Logical measurement outcomes are obtained by combining measurement outcomes of specific physical measurements. We refer here to the set of physical measurement outcomes making up a logical measurement as a *logical membrane* due to the geometric shape of its support. For example, the logical

outcome of measuring $Z \otimes Z$ on $|\psi\rangle \otimes |T\rangle$, is associated with the schematically depicted (red) logical membrane in Fig. 1 (b). This is equivalent to the single qubit Z a measurement on the second qubit which occurs after a CNOT operator in Fig. 1 (a). The membrane in Fig. 1 (b) continues towards the past and depends on the history of the two qubits. For our purpose, we may imagine that this history is summarized by two bits which accumulate the parities of the two membrane continuations.

We can decompose the lattice surgery into smaller constituent blocks which extend $\approx d$ in each direction. This is the decomposition is referred to as a *logical-block network* decomposition. The connectivity structure of this network is succinctly conveyed by a graph, with elementary blocks and their connected ports interpreted as vertices and edges respectively.

The two connected logical blocks in Fig. 1 (b) are only a fragment of the larger network for a full quantum algorithm or sub-routine. In order to provide a logical outcome, information from a set of logical blocks supporting the corresponding membrane will need to be decoded. Fig. 1 (e) partially illustrates how the support could look in terms of elementary circuit components for the example of gate synthesis using magic state injection. Fig. 1 (e) also emphasizes how quickly logical outcomes are needed to condition subsequent quantum operations. Quantum sub-routines will, in general, require *classical control* [10], i.e. using available logical outcomes to control subsequent quantum logic.

The example in Fig. 1 (e) and other quantum algorithms and subroutines involve decoding on large logical block networks with stringent requirements to enable classical control. Our modular-decoding framework allows decomposing the decoding problem into sub-tasks with the goal of enabling quick extraction of logical outcomes (i.e. fast reaction time) while retaining the low logical error rates (LER) of off-line decoders. Edge-vertex decoding, illustrated in Fig. 1 (c), is a concrete modular decoding decomposition which achieves these goals for general lattice surgery style circuits.

B. Prior work

The back-log issue was highlighted in Ref. [2], whereby decoding the entire history of the computation is impractical. They show it is possible to divide the global decoding problem into sub-decoding problems in order to get up-to-date information about the correction, even when syndrome histories involve many logical qubits. In Ref. [11], the use of parallelization is proposed to decrease the decoding time complexity. In Ref. [12], proposed using multiple decoders in parallel with message passing to reduce the reaction time.

More recently, in Refs. [13, 14], a parallel approach to decoding is proposed and numerically benchmarked, showing that decoding can be parallelized without significant impact on accuracy (LER). We note that parallel decoders for some (non-topological) quantum LDPC codes have previously been proposed [15].

Our work was developed independently, but we note partial

overlap with the recently published results in Refs. [13, 14]. Furthermore, this article makes several contributions beyond existing literature. First of all, our *edge-vertex* modular decomposition can be generally applied to arbitrary computations implemented through topological stabilizer fault-tolerance. Furthermore, the statement of modular decoding is sufficiently careful to be applicable to all known flavors of topological stabilizer computation [16], such as circuit based quantum computation, measurement-based quantum computation [17–20], fusion-based quantum computation [12] and floquet-based quantum computation [21, 22]. Finally, we prove a soundness theorem for modular decoding whose hypotheses give sufficient conditions for a sound decomposition of the decoding problem.

III. PRELIMINARIES

Classical outcomes provide the only classical window onto the quantum evolution which takes place in the computer. It is the combination of these outcomes and a physical model for operations and errors on them which will guide the fault-tolerant control and interpretation of the computation. Decoding deals with raw classical data produced during a quantum computation. These are all the outcomes from measurements performed throughout the computation, or more generally the outcomes from quantum instruments [9, 16]. We index the collection of physical outcomes of a computation by the set \mathcal{O} . For simplicity, and in anticipation of the stabilizer formalism, we will assume that outcomes take binary values denoted by $v : \mathcal{O} \rightarrow \mathbb{Z}_2$ (with $\mathbb{Z}_2 = \{0, 1\}$).

Parity checks are constraints among the measurement outcomes reflecting the redundancy among them under ideal operations (i.e., in the absence of errors). In stabilizer fault tolerance, a check σ is characterized by a sub-set of outcomes with a fixed joint parity (which we will assume to be 0 without loss of generality). By abuse of notation, extending the definition of v linearly over subsets of \mathcal{O} , we will denote this as constraint as, $v(\sigma) = 0$. A value of $v(\sigma)$ other than 0 indicates the presence of errors. We are interested in the context of stabilizer fault tolerance, where the set of all checks $\langle \Sigma \rangle$ has the structure of a linear space generated by a given set of check generators Σ (i.e., $\langle \Sigma \rangle = \text{span}(\Sigma)$). In turn, $\langle \Sigma \rangle$ is a linear subspace of the power-set $\mathcal{P}(\mathcal{O})$ of \mathcal{O} , the set of all possible subsets of \mathcal{O} which can be interpreted as the linear space $\mathbb{Z}_2^{\mathcal{O}}$ (the space of functions from \mathcal{O} to \mathbb{Z}_2). In other words, $\langle \Sigma \rangle$ is closed under *exclusive or* (XOR) of its elements (i.e., $\sigma_1 \in \langle \Sigma \rangle$ and $\sigma_2 \in \langle \Sigma \rangle$ implies $\sigma_1 \oplus \sigma_2 \in \langle \Sigma \rangle$). All the information which is relevant for the decoder to identify an error is contained in $v|_{\langle \Sigma \rangle}$ (i.e., the restriction of v to elements in $\langle \Sigma \rangle$). This information can be succinctly encoded in the resulting parities for the, possibly over-complete, generating set of checks Σ . We will assume that the decoder has access to a convenient generating set of checks Σ as well as their syndrome outcome $v : \Sigma \rightarrow \mathbb{Z}_2$ as they become available.

Although $\langle \Sigma \rangle$ encapsulates fundamental, decoder independent properties, the choice of Σ has practical importance. Check generators in Σ impact the performance of the decoder

and imprints a notion of locality which guide the decomposition of the decoding task. Some ambiguity arises when there are multiple levels (hierarchy) of encoding involved. In this situation, it is possible for check generators at a higher level to be treated as logical outcomes by a lower level fault-tolerance scheme. Magic state distillation is a practically relevant example of such a situation; there, physical injected states are unprotected by the underlying low level surface code style fault tolerance. However, the distilled magic states are nevertheless protected by higher level distillation checks.

Logical outcomes are the final product of fault-tolerant quantum computation. In the desired regime of operation, these outcomes reproduce the same value distribution as a noiseless quantum computer. Logical outcomes \mathcal{M} are derived from physical outcomes in \mathcal{O} . For stabilizer fault tolerance, logical outcomes $M \in \mathcal{M}$ take bit values. Moreover, in the absence of errors their value $v(M)$ is the joint parity of a corresponding subset of outcomes $M \subset \mathcal{O}$, which gives the ideal logical outcome distribution taken as reference. The choice of letter, \mathcal{M} , is intended to convey *membrane*, which correspond to the 2D arrangement of physical outcomes associated to logical outcomes in flavours of surface-code based fault tolerance [16].

In surface-code based flavours of fault-tolerance, logical outcomes correspond to relatively closed membranes. A membrane is relatively closed if (at some point in the computation) its support is fully contained within the set of available outcomes (i.e., it will have no support on outcomes to be generated in the future). In general, the entirety of a logical membrane is an unwieldy object, spanning and branching through (potentially the entirety of) the computation. The logical *Pauli frame* is a convenient way to tame this complexity. The Pauli frame summarizes the parity accumulated by *partial* logical membranes which may or may not, in the future, be completed into a logical outcome of \mathcal{M} . In a snapshot of the computation, there would be one partial logical membrane per element of the instantaneous n -qubit logical Pauli group (with n equal to the number of logical qubits at that instant in time); these are the bits of the Pauli frame. This approach provides the flexibility of defining the logical circuit on the go. When, completing a logical measurement (i.e., by closing a membrane M), the outcome $v(M)$ can be obtained by taking a joint parity of the *historic* parity of M , as given by a corresponding Pauli frame element with a *recent* term associated to the closure of M . Partition of historic and recent is arbitrary but serves a practical purpose.

For ideal noiseless operations, each bit of the Pauli frame simply accumulates the partial outcome parity for some partial membrane M . In noisy fault-tolerant computation, this parity may require adjusting in order to compensate the effect of diagnosed errors on the logical Pauli frame.

Error model. In a real-world device, operations are not perfect, and so the observed outcome distribution differs from the ideal one. Fault-tolerant schemes can deal with such imperfections contingent on an adequately benign noise model. Soundness proofs and numerical simulations in this and other articles assume such noise models, which are themselves an idealization. While in this way, we gain confidence that fault-

tolerance is capable of producing robust computational outcomes, the final validation will only come with an actual fault-tolerant computation.

As in most stabilizer fault-tolerance literature, we assume an error model defined in terms of a set of elementary *errors* or faults $e \in \mathcal{E}$ which are Pauli (product) operators acting on the qubits at different times throughout the computation. This choice is motivated by the fact that for stabilizer fault-tolerance, wherein the (Pauli) measurements used to generate the parity checks collapse many coherent errors into Pauli errors, and thus the effects of a wide range of errors can be modeled in this way. The choice of elementary errors \mathcal{E} is model specific and should aim to represent the physics and imperfections of the device(s) being modeled.

A common choice of error generators \mathcal{E} , is to have a one to one relation between physical measurement outcomes $o \in \mathcal{O}$ and each error generator $e \in \mathcal{E}$, with each element e flipping a single outcome o . While this can be an adequate model certain implementations of MBQC or FBQC, it actually conflates two distinct objects and can not accurately model many other scenarios. To comply with the format accepted by a concrete decoding algorithm (e.g., syndrome graph structure, *i.i.d.* error model), the internal decoder error model may in turn be an approximation of the mathematical error model. For simplicity, we do not distinguish them here.

We denote by $\langle \mathcal{E} \rangle$, the possible combinations of elementary errors in \mathcal{E} , and will use $\epsilon \in \langle \mathcal{E} \rangle$ to denote the unknown error combination occurring on the quantum system. We further assume that the probability of different errors $\epsilon \in \langle \mathcal{E} \rangle$ occurring can be described by an independent probability distribution (or possibly a low correlation distribution) on elementary error generators $e \in \mathcal{E}$.

In a quantum instrument network (QIN), composed of stabilizer instruments (a generalization of Clifford maps including measurement) [9], the effect of inserting Pauli errors between instruments is to flip a set of outcomes. Specifically, there is a linear relation which determines which checks $\sigma \in \langle \Sigma \rangle$ and logical membranes $M \in \mathcal{M}$ are flipped by a given error $\epsilon \in \langle \mathcal{E} \rangle$. We denote this relation by the bi-linear map ∂ , with $\partial\epsilon : \langle \Sigma \rangle \rightarrow \mathbb{Z}_2$, along with $\epsilon_{\mathcal{M}} : \mathcal{M} \rightarrow \mathbb{Z}_2$, which are themselves linear in $\epsilon \in \langle \mathcal{E} \rangle$. Thus, a specific error ϵ flips a well defined set of logical outcomes specified by the indicator function $\epsilon_{\mathcal{M}}$; the problem we are faced with is to identify which these are without knowing ϵ .

Decoding consist of accurately inferring $\epsilon_{\mathcal{M}}$ by using the prior distribution of ϵ as well as its signature over the available syndrome information $\partial\epsilon = v|_{\Sigma}$. In practice, decoders approach this problem by inferring a recovery operator κ which also belongs to $\langle \mathcal{E} \rangle$. As such, it also has associated linear maps $\partial\kappa$ and $\kappa_{\mathcal{M}}$. The decoder will be successful if it can identify a correction κ such that $\kappa_{\mathcal{M}} = \epsilon_{\mathcal{M}}$. Note that this is a much weaker requirement than $\kappa = \epsilon$, which is not necessary for successful decoding. However, since decoders do not have access to $\epsilon_{\mathcal{M}}$ they pick a recovery operator κ with relatively high likelihood such that $\partial\kappa = \partial\epsilon$ (i.e., the recovery operator κ has exactly the same syndrome as the error ϵ). In other words, applying the combination of error ϵ and recovery κ leads to all parity checks in Σ being satisfied (i.e., the trivial

syndrome). Note however, that only $\kappa_{\mathcal{M}}$ and not the entirety of κ is the relevant information produced by the decoder. In a real-time decoding process, this allows efficiently summarizing partial decoding progress by keeping track of the effect of κ on partial membranes with an error-corrected Pauli frame.

ϵ : the physical error configuration.

κ : the global correction chosen by the decoder.

Fault distance is an important quantity characterizing the noise resilience of a fault-tolerant protocol. It depends only on the error generators \mathcal{E} and its relationship with the logical outcomes \mathcal{M} and the space of checks Σ but is independent of the decoder.

We say that an error $\epsilon \in \langle \mathcal{E} \rangle$ is undetectable, if it has a trivial syndrome (i.e., $\partial\epsilon = 0$). The weight of an error operator $\epsilon \in \langle \mathcal{E} \rangle$, denoted by $|\epsilon|$, is the smallest number of elementary faults $e \in \mathcal{E}$ needed to express ϵ (i.e., as $\epsilon = e_1 e_2 \dots e_{|\epsilon|}$). The fault distance d of a protocol, is the weight of the smallest non-trivial undetectable error (i.e., the smallest $|\epsilon|$ such that $\partial\epsilon = 0$ but $\epsilon_{\mathcal{M}} \neq 0$). In other words, it is the weight of the smallest undetectable error giving rise to a change in a logical measurement outcome.

Note that the weight is dependent on the error model of interest through the set of elementary error generators \mathcal{E} . If a decoder with *effective fault distance* of d over a fault-tolerance protocol, can **detect** any error of weight up to $d - 1$ and can **correct** any error with weight up to $\lfloor \frac{d-1}{2} \rfloor$. A *decoder is sound* w.r.t. a fault-tolerant protocol with fault distance d , iff the decoder also has an effective fault distance d .

Definition 1. [Decoder soundness] The decoder produces a minimum weight correction κ for any (physical) error ϵ with $|\epsilon| < d/2$, where d is the fault distance of the protocol.

This means that a decoder satisfying the soundness condition will correctly recover from any physical error configuration $\epsilon \in \langle \mathcal{E} \rangle$ with $|\epsilon| < d/2$. MWPM [2, 23] and UF [24] are sound decoders w.r.t. any fault tolerant protocol as long as the relation ∂ between error generators \mathcal{E} and check generators Σ is accurately captured by a *syndrome graph*.

Syndrome graphs are a useful data structure to represent the decoding problem whenever each elementary error $e \in \mathcal{E}$ flips at-most two parity checks $\sigma \in \Sigma$. This leads to a graph structure with check generators Σ corresponding to vertices of the graph and elementary errors $e \in \mathcal{E}$ flipping a given pair of check generators corresponding to edges between corresponding the vertices of the graph. One can define syndrome graphs for simple *i.i.d.* Pauli and measurement error models for circuit-based quantum computation (CBQC) with the surface code [2, 25–28], measurement-based quantum computation (MBQC) with topological cluster states [17–20], or fusion-based quantum computation (FBQC) with the 6-ring fusion network [9, 12, 29]). While our numerical implementation and simulation results (Sec. VII) make use of the syndrome graph structure, our modular decoding decomposition approach and proof (Sec. V) are applicable more broadly to Tanner graphs with locality structure.

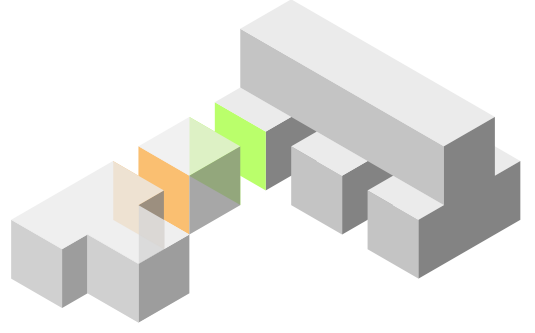


FIG. 2. Logical blocks and logical-block network. From left to right, there are the 3-port block, identity, and lattice surgery logical blocks. By matching the ports (colored surfaces) of these blocks, we arrive at a logical-block network.

Connected error clusters: The check generators Σ and error generators \mathcal{E} together with their anti-commutation relations ∂ define a Tanner graph. This is a bipartite graph with each node representing either a check generator $\sigma \in \Sigma$ or an error generator $e \in \mathcal{E}$ and edges between them used to represent the relation $\partial e(\sigma) = 1$. We will say that two error generators e_1 and e_2 are *directly connected* if they are distance 2 in the Tanner graph (i.e., there is at least one check generator σ s.t. $\partial e_1(\sigma) = 1$ and $\partial e_2(\sigma) = 1$).

Given an error configuration ϵ we may use this notion of *connectedness* to partition it into *connected components*. We will call each of these components a *connected error cluster*. In the case of syndrome graphs, this notion coincides with viewing ϵ as a sub-graph (subset of edges) of the syndrome graph and identifying its connected components. The rationale behind this definition is that if $\partial\epsilon = 0$ and ϵ has connected components ϵ_i , then $\partial\epsilon_i = 0$. In other words, an error configuration ϵ is undetectable, if and only if, all of its connected components are undetectable. For this reason, lowest weight undetectable logical errors will always consist of a single connected error cluster.

Surface code fault-tolerant protocols. Our primary interest, is on fault-tolerant protocols based on the surface-code. In this case, a quantum computation is expressed as a network of logical operations, which we call a *logical block network* following Ref. [9]. Each element in the network is a logical block—an encoded, logical operation realized by a *quantum instrument network (QIN)* along with some input and output ports for the logical information. Specifics depends on the operations being implemented, as well as the model of computation (CBQC, MBQC, or FBQC) [16]. The native physical instruments used: unitary gates, single qubit measurements, two-qubit parity measurements, resource state generation, and any other operations depend on which model of computation is best suited to the underlying physical hardware. Blocks are composed along ports to generate larger computations, with a schematic example depicted in Fig. 2. Regardless of the model, the connectivity structure of surface code QINs locally follow a 3-dimensional network representing the space-time history, and both outcomes and topological checks are local-

ized in this structure. For example, surface code computations using lattice surgery [7–9], or ZX-spider networks [9, 30, 31] generate 3D networks like those depicted in Fig. 2. We explain these logical blocks in more detail in Sec. VI.

IV. MODULAR DECODING METHODS

A logical block network defines a class of decoding problems $(\Sigma, \mathcal{M}, \mathcal{E})$, with their relation ∂ and possibly a probability distribution over $\langle \mathcal{E} \rangle$. A specific problem instance, is given by the syndrome configuration $\partial\epsilon$ corresponding to a physical error $\epsilon \in \langle \mathcal{E} \rangle$. In this section, we show how to divide the decoding problem of a network (or part of one) into smaller decoding sub-tasks, which can be solved separately—some in parallel—and then combined to solve the global problem.

A. Decomposing the decoding problem

Modular decoding acknowledges that the entirety of the decoding problem will only be available once the quantum algorithm is completed. It addresses the problem of providing logical outcomes throughout the computation by splitting the monolithic problem into decoding sub-tasks of manageable size. The solution to each sub-task includes a portion of the global recovery κ . Crucially, these tasks can begin as soon as their input data is available. Furthermore, as soon as the necessary outcomes and portions of κ are available *error corrected logical outcomes* $\bar{v}(M) := v(M) \oplus \kappa_{\mathcal{M}}(M)$ can be computed. This allows the quantum computation to perform feed-forward classical control wherein the logical block structure of the computation changes depending on the extracted classical outcomes.

A *recovery-based decoder* proceeds by finding a recovery operator $\kappa \in \langle \mathcal{E} \rangle$, with the property $\partial\kappa = \partial\epsilon$. The approach taken by modular decoding is to split this problem into decoding sub-tasks indexed by $i \in \mathcal{T}$, with each task committing a portion κ_i of the global correction κ

$$\kappa := \sum_{i \in \mathcal{T}} \kappa_i. \quad (1)$$

How is each component κ_i obtained? Each decoding task $i \in \mathcal{T}$ is defined by its own set of check generators $\Sigma_i \subseteq \Sigma$, and error generators $\mathcal{E}_i \subseteq \mathcal{E}$. The check generators Σ_i and error generators \mathcal{E}_i defining different decoding tasks can partially overlap in general.

$\epsilon_i \in \langle \mathcal{E}_i \rangle$: the portion of the physical error configuration relevant to decoding task $i \in \mathcal{T}$.

$\mu_i \in \langle \mathcal{E}_i \rangle$: a correction estimate produced by task $i \in \mathcal{T}$.

$\kappa_i \in \langle C_i \rangle$: the portion of the correction estimate μ_i committed as part of the global correction κ by task $i \in \mathcal{T}$.

The result of each decoding task i is a recovery estimate $\mu_i \in \langle \mathcal{E}_i \rangle$. Crucially, not all of the correction operator μ_i is

taken at face value and committed into the final correction κ . Only the restrictions of recovery estimate μ_i to the smaller commit region C_i are used to determine the final correction κ . Having a sufficient buffer is essential to maintaining good decoding performance, as otherwise the low-weight errors may lead to logical faults. We refer to this problem as a reduction in the *effective fault distance*. Examples of how the effective decoding distance may be halved in the absence of buffers are shown in Fig. 3.

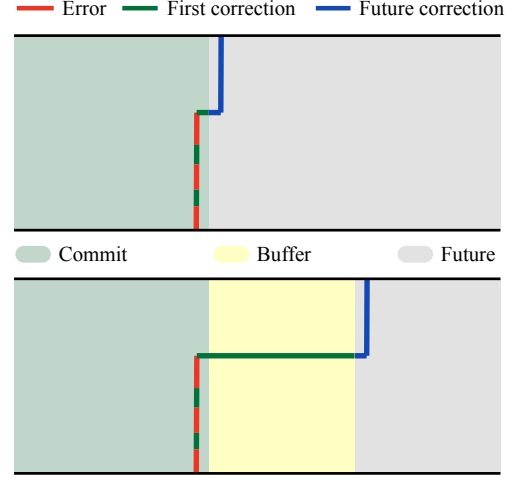


FIG. 3. (upper panel) Distance reduction of vanilla modular decoding with no buffer. In a first stage, an error with weight $\approx d/4$ (red) results in an miss-leading partial correction (green line). This leaves an updated syndrome which leads further decoding to complete a logical error (blue line). (lower panel) The same error configuration is presented. In this case, the first decoder is aware of additional buffer of syndrome information (yellow region). A similarly misleading correction (green) is no longer viable for the local decoder as it has higher weight than the actual error.

The global recovery operator κ is obtained by taking portions κ_i of these recovery estimates μ_i (i.e. $\kappa|_{C_i} = \kappa_i := \mu_i|_{C_i}$).¹ The *commit regions* C_i partition the full set of error generators \mathcal{E} into disjoint subsets

$$\mathcal{E} = \bigcup_{i \in \mathcal{T}} C_i. \quad (2)$$

In turn, each commit region $C_i \subseteq \mathcal{E}_i \subseteq \mathcal{E}$ is a subset of the error generators \mathcal{E}_i relevant to decoding task i , with

$$\mathcal{E}_i = C_i \cup B_i. \quad (3)$$

The remaining set of error generators $B_i := \mathcal{E}_i \setminus C_i$ relevant to each decoding task is called the *buffer region* for task i and improves the quality of κ_i .

¹ Here, the operator $|$ denotes the restriction operator with respect to a specific subset of error generators and assumes a unique representation of the original element being restricted in terms of error generators.

B. Data dependency among sub-tasks

In order to obtain a consistent recovery operation κ such that $\partial\kappa = \partial\epsilon$ decoding tasks will need to communicate. In particular, there are check generators $\sigma \in \Sigma$ which straddle two (or more) commit regions C_i, C_j (i.e., there exists error generators $e_i \in C_i$ and $e_j \in C_j$ such that $\partial e_i(\sigma) = 1$ and $\partial e_j(\sigma) = 1$). Decoding of these tasks will need to coordinate to guarantee $\partial(\kappa_i + \kappa_j + \epsilon)(\sigma) = 0$. We call decoding tasks $i, j \in \mathcal{T}$ sharing such a check *neighbours* and must somehow communicate.²

We assume that communication between tasks is exclusively achieved by adapting the input instance of some tasks based on the outputs/solutions obtained for other tasks. This preserves the functional input-output signature assumed from off-the-shelf decoding algorithms. This precludes neighbouring decoding tasks from being solved in parallel (otherwise their combined recovery may not satisfy checks straddling both commit regions). As such, a sequential causal order is introduced between all neighboring decoding tasks; the order of which is a design choice we study in section VI.

The assumed causal order between decoding tasks can be modelled with a *scheduling graph* $G_{\text{sch}} := (\mathcal{T}, \prec)$. This is a directed, acyclic graph (DAG), with vertex set given by \mathcal{T} (i.e., one vertex per decoding task). A directed edge is placed between each pair of neighboring tasks $i \prec j$ with the direction denoting the dependence of the input of j on the output of i . Tasks can only be consistently ordered if the graph is acyclic (i.e., not have directed cycles). The scheduling graph can partly determine the reaction time—the computational contribution to the reaction time is upper bounded by the depth of the scheduling graph multiplied by the (maximal) time taken for a sub-decoder to return a recovery. We will discuss scheduling schemes in Sec. VI.

The set of visible syndromes, provided as input for a decoding task j , may be altered based on the output from other decoding tasks i preceding it ($i \prec j$). In particular, instead of the syndrome $\partial\epsilon$ which only includes the effect of the physical errors ϵ , the input instance to decoder j will consist of the syndrome $\partial(\epsilon + \kappa_{P_j})$, where $\kappa_{P_j} := \sum_{i \prec j} \kappa_i$ includes the corrections committed by all prior decoders. In practice, Σ_j will not include check generators which are already guaranteed to be trivial for $\kappa_{P_j} + \epsilon$ and only a small number of check generators in Σ_j will be affected by corrections in neighboring tasks and will need to have their syndrome updated in the input to task j . As illustrated in Fig. 4, this can be viewed as setting a boundary condition for task j .

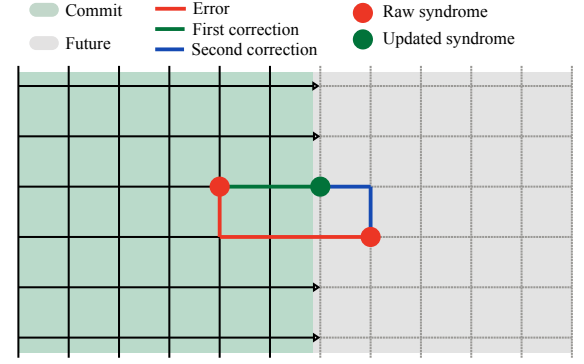


FIG. 4. The square lattice represents a syndrome graph, with vertices as check generators Σ and edges as error generators \mathcal{E} that flip the checks they are incident to. The green and grey shading illustrates a partitioning of the decoding problem into two sub-tasks L (left) and R (right). Errors ϵ (red lines) can span multiple components with the syndromes $\partial\epsilon$ (red dots) possibly spread accordingly. Error generators at the interface, represented by arrow edges, affect checks in both Σ_L and Σ_R . They are included in C_L , a subset of the error generators \mathcal{E}_L for the component which is decoded first. Doing so guarantees satisfying all check generators $\sigma \in \Sigma_L$ (vertices in the green shaded region) regardless of the future corrections κ_F . However, the committed correction κ_L (green line) also produces an *updated syndrome* $\partial(\epsilon + \kappa_L)$ which may be different from $\partial\epsilon$ along the interface, as illustrated by the green dot. The second decoding sub-task takes this updated syndrome $\partial(\epsilon + \kappa_L)$ as input to produce a second correction component κ_R (represented by the blue line). Buffers are not illustrated as they are not necessary to illustrate the notion of residual syndrome and data dependency.

C. Logical outcomes from partial membranes and corrections

For each commit region C_i a sub-decoder commits a fragment κ_i of the global recovery $\kappa \equiv \sum_{i \in \mathcal{T}} \kappa_i$. In particular, the recovery's effect on logical membrane M is given by the map $\kappa_{\mathcal{M}}(M) = \sum_{i \in \mathcal{T}} \kappa_i \mathcal{M}(M)$. A specific membrane $M \in \mathcal{M}$ can only have a finite subset of tasks $\mathcal{T}(M) \subseteq \mathcal{T}$ which can ever contribute to this sum (an intuitive reason for this is that outcomes are not affected by later errors). We call this subset the *relevant tasks to M* and denote it by $\mathcal{T}(M) := \{i \in \mathcal{T} | \exists e \in C_i : e_{\mathcal{M}}(M) \neq 0\}$. Once all outcomes for M are available and relevant decoding tasks completed, the corrected logical outcome for M can be determined by the (mod 2) sum of all partial membranes across the commit regions,

$$\bar{v}(M) := v(M) + \sum_{i \in \mathcal{T}(M)} \kappa_i \mathcal{M}(M), \quad (4)$$

where $\bar{v}(M)$ denotes the *error corrected outcome* for M . We will in general assume that the uncorrected outcome $v(M)$ can also be decomposed into partial membrane contributions along a similar partition.

² Note that this notion is dependent on the specific choice of check generators Σ and error generators \mathcal{E} . For topological fault-tolerant schemes, there is often a natural set of *low-weight* generators which involve a small number of outcomes and detect a small number of error generators.

D. Buffer growth

To keep the decoding tasks small and reaction time as low as possible, the size of the decoding sub-tasks must be as small as possible without impacting decoding quality. However, the theorem proved in section V as well as the numerical result of section VII support the qualitative conclusion drawn from Fig. 3 and other examples. Namely, a buffer region of width $b \geq d$ (or close to it) is needed to maintain the decoding quality of monolithic decoding in a modular decoding approach. In this section, we describe how minimal buffer regions $B_i := \mathcal{E}_i \setminus C_i$ as well as the set of relevant check generators Σ_i for each decoding task $i \in \mathcal{T}$ can be obtained extracted automatically. The only input needed is the partition of \mathcal{E} into commit regions C_i , the desired buffer distance b and the partial order \prec among decoding tasks.

From each commit region C_i , a graph traversal (breadth first search) is performed into other error generators of \mathcal{E} . The graph structure used is the neighbor relation induced by the check generators Σ . However, error generators in P_i are not included in the growth phase. This graph traversal collects all error generators at a graph-distance smaller or equal than a predefined buffer size b and adds them to B_i if they don't already belong to C_i . Since P_i does not participate in the graph traversal, past commits act as a barrier to the buffer growth. As such, error generators which are a short distance from C_i in the full syndrome graph (or Tanner graph), may end up being excluded due to past commits in P_i .

The same growth process can also be used to identify the check generators Σ_i , which should be actively considered in the decoding task. The check generators in Σ_i are those whose syndrome is fully determined by $P_i \cup C_i \cup B_i$ and not fully determined by P_i . Note that by definition, the growth phase does not proceed into P_i and check generators whose syndromes are fully determined by P_i should already be neutralized by previous commits κ_{P_i} .

E. Summary: modular decoding anatomy

We now summarize the various components of a modular decoding problem. A global decoding problem can be divided into several, modular decoding sub-tasks, each of which will in general only have access to partial information. From the perspective of each sub-task $i \in \mathcal{T}$, the global set of error generators \mathcal{E} is partitioned into four distinct regions.

P_i : The subset of errors generators ($P_i \subseteq \mathcal{E}$) for which a correction has already been committed in the **past**.

C_i : The subset of error generators ($C_i \subseteq \mathcal{E}$) for which the current decoder will **commit** the final correction κ_i .

B_i : The current decoder will solve the decoding problem with respect to a larger subset of error generators $\mathcal{E}_i \equiv C_i \cup B_i$. The subset B_i is treated as a **buffer** to improve the decoding quality in C_i . The B_i component of the

correction estimate μ_i will be discarded or revised later.

F_i : The subset of error generators ($F_i \subseteq \mathcal{E}$) from the **future**, which have no influence on visible check generators.

The decomposition into these components is central in the soundness proof of modular decoding provided in section V. Our approach to specifying the decomposition of modular decoding into sub-tasks will be to start from a partition of the error generators \mathcal{E} into commit subsets C_i . To do so, we will mirror the logical block decomposition of the circuit. At this point one of a few sensible schedules G_{sch} discussed in section VI can be chosen to provide a data dependency structure among decoding tasks. Finally, the P_i , and the buffer regions B_i can be obtained algorithmically given a target buffer size b (see IV D), which should be chosen as $b \approx d$.

In addition to this partition of the error generators, it is sometimes necessary to connect to the actual set of physical measurement outcomes V_i , which are in principle available to a given decoding task.

V_i : The **visible** subset of outcomes ($V_i \subseteq \mathcal{O}$) which are *in principle* available to the current decoder task i . These typically includes past outcomes which are no longer directly relevant to the current decoding task.

In practice, the input to a decoding task instance is based on syndromes and syndromes are based on outcomes. It will be sufficient to assume that V_i is the smallest subset of outcomes \mathcal{O} supporting the check generators in Σ_i and any Σ_j with $j \prec i$. In practice however, many of the check generators in Σ_{V_i} are already guaranteed by κ_{P_i} and are not influenced by error generators in $B_i \cup C_i$ so it is sufficient for the local decoding task to focus on Σ_i .

When we are dealing with a setting where there is a one to one correspondence between error generators and outcomes, the *visible* region is specified by $V_i = P_i \cup C_i \cup B_i$. Based on our algorithmic construction of B_i and Σ_i from Sec. IV D, we may interpret Σ_{V_i} to be a maximal subset of check generators unaffected by error generators in F_i , and V_i the minimal subset of outcomes supporting said checks. The practical importance of V_i , is that the decoder unit responsible for task i needs to wait for said outcomes to be available before it can begin solving its task.

V. MODULAR DECODING WITH BUFFERS: PROOF OF DECODER SOUNDNESS

In this section, we prove that modular decoding is sound. Namely, we show that, under two assumptions, it can achieve an effective fault distance d equal to the fault distance of the original decoding problem.

The first assumption, is local **decoder soundness**, which is a requirement on the base decoding algorithm used to obtain corrections for individual decoding sub-tasks, as was defined

in Def. 1. We recall that some decoders in the literature such as MWPM [2, 23] and UF [24] satisfy this property; these are good candidates to use as local decoders.

The second assumption, constrains the size/shape of the commit and buffer regions used to define individual decoding sub-tasks. It goes by the name of *buffering condition*, and is stated as follows:

Definition 2. [Buffering condition] For a decoding sub-task with buffer, any connected errors ϵ satisfying the following conditions will have weight d or larger.

- ϵ is supported on $C \cup B$
- ϵ is undetectable in the visible region ($\partial_V \epsilon = \emptyset$).
- ϵ has support in the commit region ($\epsilon_C \neq \emptyset$).
- ϵ is detectable globally ($\partial \epsilon \neq \emptyset$).

See Fig. 5 for examples of error clusters which satisfy (or not) the itemized buffering conditions.

Note that throughout this section, the index $i \in \mathcal{T}$ for the current decoding task is kept implicit throughout the inductive proof. We nevertheless use the labels P , C , B and F as in section IV, to refer to the partition of error generators \mathcal{E} into past, commit, buffer and future from the perspective of i . The decoder in charge of a decoding task has access to outcomes in $V \subseteq \mathcal{O}$ at best. Consequently, instead of the full syndrome ∂ it only has access to a partial syndrome ∂_V corresponding to those check generators supported exclusively on visible outcomes V . We will assume that V is the minimal set of outcomes supporting all check generators which are unaffected by errors in F . In other words, V supports all check generators $\sigma \in \Sigma$ whose syndrome is fully determined by the error restriction to $P \cup C \cup B$.

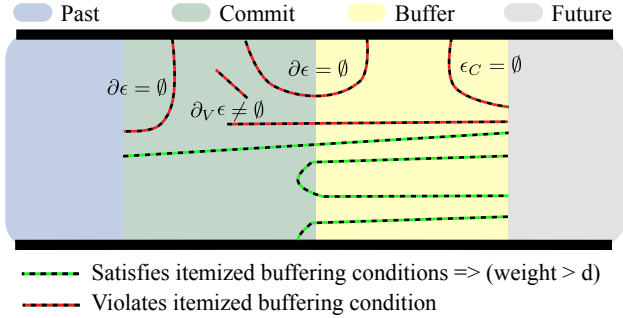


FIG. 5. The figure illustrates a collection of error strings (connected error clusters) supported on $B \cup C$. The buffering condition (Def. 2) states that low weight error clusters satisfying certain *itemized requirements* should not exist. Error clusters which satisfy itemized conditions (dashed green black), must have weight larger than d for the buffering condition to be satisfied. The ones that do not satisfy itemized conditions (dashed red black) may have lower weight. For these, formulas identify which of the three *itemized requirements* is not fulfilled.

While the buffering condition is expressed in terms of an arbitrary error ϵ , in the soundness proof the condition is applied to specific combinations of errors and corrections. These

combinations are constructed to be “locally neutral” as they combine a decoder-generated recovery operation with its instigating error.

The buffer growth method in Sec. IV D (with $b := d$) generates decoding regions which satisfy the buffering condition. If we use d as the buffer depth, then no error cluster with weight smaller than d can have support on both the commit C and future F , because errors from these two regions have graph-distance larger than d . This is guaranteed by the graph traversal approach used to determine B .³

Theorem 1 (Modular decoding theorem). *If at every step of modular decoding (i.e., for every decoding sub-task) the buffering condition and local decoder soundness are satisfied, then the overall modular decoding procedure satisfies the soundness condition.*

Informal argument: Intuitively, the buffering condition means that any *connected* error cluster with weight smaller than $d/2$ which is partially supported on the commit region, (C) must be fully supported on commit + buffer ($C \cup B$). Because otherwise a “round trip” of this string that is undetectable in commit + buffer, has two open ends in the (non-buffered) future, and has weight smaller than d – violating the buffering condition. As a result, the local decoder will provide the correct recovery (say, a string from points x to z), but only apply the component in the commit region (a string from points x to y). The missing part (a string from y to z) will be completed by the following sub-decoders, because if the minimum weight path from x to z is through y , then the minimum weight path from y to z has the same weight as the yz -segment on the xy -path.

We will continue to use Greek letters to describe error strings and correction candidates. These will further proliferate in the proof of modular decoding soundness so we pre-emptively summarize their interpretations in table I.

TABLE I. Symbol key: errors and recovery operators

| | |
|----------------|--|
| ϵ : | the physical error configuration. |
| κ : | the global correction the modular decoder commits to. |
| μ : | the correction estimate proposed for the current decoding task $C \cup B$. ($\mu \equiv \mu_{CB}$). ($\kappa_C \equiv \mu_C$). |
| τ : | a processed portion of the errors ϵ reliably addressed by the previous correction estimates. ($\tau \subseteq \epsilon$). ($\tau_P \equiv \epsilon_P$). |
| ν : | a viable low-weight correction candidate for τ compatible with previous commits (ignores $\bar{\tau}$). |
| $\bar{\tau}$: | an unprocessed portion $\bar{\tau} := \epsilon - \tau$ of the errors ϵ . |

Whereas the proof applies generally, to stabilizer fault-tolerance with some notion of locality, our intuition is derived

³ The graph structure used is derived from the elementary error generators of $\mathcal{E} \setminus P$ and the elementary check generators Σ .

from syndrome graph type decoding problems, for which Fig. 6 can further illustrate the elements involved in the proof.

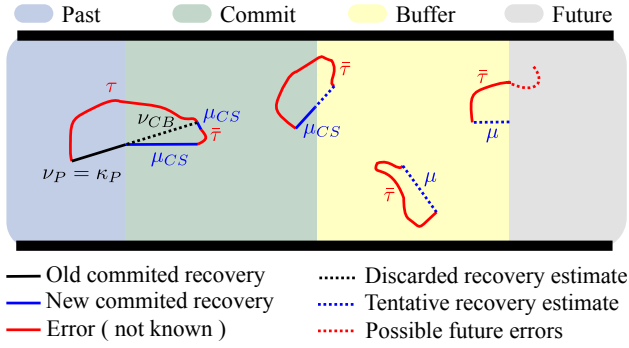


FIG. 6. An illustrative configuration of the different regions as well as error and correction chains. Errors and corrections are labeled by Greek letters following Sec. I. Here, the *decoding causal order* is presented from left to right whereas in general the order is decoupled from the particular geometric coordinates of the decoding problem. The error ϵ (red lines) is partitioned into a processed component τ , which can be compensated by a lower weight correction $\nu = \nu_P + \nu_{CB}$, and the unprocessed error $\bar{\tau} = \epsilon - \tau$. The unprocessed error $\bar{\tau}$ affecting visible outcomes can be decomposed into connected components, some of which will share support with the current commit region C . The recovery estimate μ produced for the current decoding task contains μ_{CS} , the parts which the proof deems as necessarily trustworthy, including the correction $\mu_C := \mu_{CS} \cap C$ to be committed. Sub-optimal correction estimates in parts of μ disconnected from C are less harmful to the global decoding quality, as these will be revised with the benefit of future information. Note after this step, the past region P grows to include the current commit C , and the committed correction κ_P will be extended with μ_C .

In the context of the current decoding task, κ_P is already defined and corresponds to past committed error estimates. The available syndromes of the error are given by $\partial_V \epsilon$. The decoder returns a correction estimate μ with

$$\mu_{CB} \equiv \mu, \quad \partial_V \mu = \partial_V (\kappa_P + \epsilon_V).$$

The global correction is committed for region C as $\kappa_C := \mu_C$.

Notice that the decoder might need to **abort** if there is no error estimate μ which is local to $C \cup B$, $\mu \equiv \mu_{CB}$, and is compatible with the error ϵ and previously committed estimate κ_P , $\partial_V \mu = \partial_V (\kappa_P + \epsilon)$. This is also a decoding failure, and is taken into account below.⁴

Proof. The strategy is to show inductively that, assuming $|\epsilon| < d/2$, at every step there exist τ and ν such that the following condition is satisfied⁵,

$$\tau \subseteq \epsilon, \quad \tau_P = \epsilon_P, \quad \nu_P = \kappa_P, \quad |\nu| \leq |\tau|, \quad \partial \nu = \partial \tau.$$

Within the inductive proof, τ can be considered as a fragment of the error ϵ already dealt with. Conversely, ν is a viable

extension of the committed correction κ_P into a viable global correction for ϵ . Neither of these have a physical (or programmatic) counterpart, and only play a role in the proof.

This is enough because when it holds after the last step then $|\kappa| \leq |\epsilon|$. Each inductive step corresponds to a decoding task which is performed, and the order in which such steps are taken in the proof can be any complete order compatible with the causality relation \prec imposed on decoding tasks.

For the base case of the induction, it suffices to take $\tau = \nu = 0$. For the inductive step, assume that indeed we have such ν, τ . The aim is to construct some ν', τ' satisfying the required conditions after the modular decoding step (i.e., $P \mapsto P \cup C$). Let

$$\bar{\tau} := \epsilon - \tau.$$

The modular decoding step produces some $\mu = \mu_{CB}$ satisfying

$$\begin{aligned} \partial_V \mu &= \partial_V (\kappa_P + \epsilon_V) = \partial_V (\nu_P + \tau_P + \epsilon_{CB}) \\ &= \partial_V (\nu_{CB} + \tau_{CB} + \epsilon_{CB}) = \partial_V (\nu_{CB} + \bar{\tau}_{CB}). \end{aligned}$$

(The existence of μ is a consequence of the rightmost expression.) The correction μ has minimal weight by virtue of *decoder soundness*, since

$$|\bar{\tau}_{CB} + \nu_{CB}| \leq |\bar{\tau}| + |\nu| \leq |\bar{\tau}| + |\tau| = |\epsilon| \leq d/2.$$

Consider a region S obtained as the union of the *support* of those connected components of

$$\alpha := \mu + \bar{\tau}_{CB} + \nu_{CB}$$

that contain some element of the commit region C . Since $\partial_V \alpha = 0$ we have $\partial_V \alpha_S = 0$, that is

$$\partial_V \mu_S = \partial_V (\bar{\tau}_S + \nu_S).$$

and μ_S has to be optimal itself, so that

$$|\mu_S| \leq |\bar{\tau}_S| + |\nu_S|,$$

The buffering condition applies to each connected component of α_S and thus $\partial \alpha_S = 0$, i.e.,

$$\partial \mu_S = \partial (\bar{\tau}_S + \nu_S).$$

Let $C \cup S$ be the region obtained as the union of S and region C . Clearly $\alpha_S = \alpha_{CS}$ and thus

$$|\mu_{CS}| \leq |\bar{\tau}_{CS}| + |\nu_{CS}|, \quad \partial \mu_{CS} = \partial (\bar{\tau}_{CS} + \nu_{CS}).$$

We take

$$\nu' := \nu + \nu_{CS} + \mu_{CS}, \quad \tau' := \tau + \bar{\tau}_{CS}$$

and it suffices to check that

$$\begin{aligned} \tau' &\subseteq \epsilon, \quad \tau'_C = \epsilon_C, \quad \nu'_C = \kappa_C, \\ |\nu'| &\leq |\tau'|, \quad \partial \nu' = \partial \tau'. \end{aligned}$$

⁴ In practice, the syndrome for $\Sigma_i \subseteq \Sigma_V$, which excludes checks generators already guaranteed by κ_P is enough (see Sec. IV). Since $i \in \mathcal{T}$ is kept implicit here, we use Σ_V to distinguish from Σ .

⁵ Notation: binary vectors are identified with set through indicator vectors.

Indeed:

$$\begin{aligned}
\tau' &= \tau + \bar{\tau}_{CS} \subseteq \tau \cup \bar{\tau} = \epsilon, \\
\tau'_C &= \tau_C + (\bar{\tau}_{CS})_C = \tau_C + \bar{\tau}_C = \epsilon_C, \\
\nu'_C &= \nu_C + (\nu_{CS})_C + (\mu_{CS})_C \\
&= \nu_C + \nu_C + \mu_C = \mu_C = \kappa_C, \\
|\nu'| &\leq |\nu| - |\nu_{CS}| + |\mu_{CS}| \leq |\tau| + |\bar{\tau}_{CS}| = |\tau'|, \\
\partial\nu' &= \partial(\nu + \nu_{CS} + \mu_{CS}) = \partial\tau + \partial\bar{\tau}_{CS} = \partial\tau'. \quad \square
\end{aligned}$$

A. Modular decoding with erasures

In a Pauli noise model each error in $\langle \mathcal{E} \rangle$ occurs according to a certain probability distribution (usually described by an *i.i.d.* model over the generators \mathcal{E}). The control software must get any information about which error actually happened from the extracted syndrome. In contrast, for an error model including erasures, there is additional information available. Rather than having an outcome be flipped with some probability and only be able to infer whether the outcome was flipped or not from syndrome information, some outcome may be flagged as *erased*. This information is provided by *herald outcomes*, which go beyond the Z_2 linear structure of checks and logical outcomes. Rather than a probability distributions over Pauli faults, a noise model including erasure can be seen as a conditional distributions of Pauli faults conditioned on the sample drawn from a probability distribution of erasures.

Traditionally, each erasure correspond to a missing measurement outcome. An outcome o which is flagged as erased may be assigned an arbitrary *guess value* $v(o)$. This corresponds to having an error generator $e_o \in \mathcal{E}$, which corresponds to a measurement error on o and is modeled to occur with 50% probability whenever the erasure is heralded for o .

A decoder which is aware of an erasure flag on o , will not take the value $v(o)$ seriously. In fact, this value may be missing from the input and can be generated at random by the decoder itself, and reassign its value if the initial guess is otherwise deemed incompatible with the most likely error configuration.

In this sense, erasure is a more benign form of noise than flip noise since an outcome flip probability $p/2$ is equivalent to an outcome erasure probability of p where the herald information (i.e., which outcomes were erased) is ignored. Furthermore, if erasures are the only form of noise, exact decoding can be performed wherein logical outcomes are either correctly recovered or lost in a heralded way. A fault tolerant stabilizer protocol which has fault distance d w.r.t. a Pauli error model will also be able to perfectly recover from up to $d - 1$ erasures w.r.t. the same error generators.

We may apply the soundness proof of modular decoding to a *post-erasure* fault-tolerance protocol. In other words, we can seek to partition a decoding problem on which erasures have already been taken into account. Once the erasures are taken into account one is left with a decoding problem with distance $d' \leq d$ the conditional Pauli error distribution over a subset of the remaining error generators. The modular decoding theorem need only be applied to distance d' , requiring

less buffering. However, the decoding problem resulting from including the erasure instance will also be *less local*. Check generators affected by a shared erasure will be considered as being at distance zero from each other.

Applying the modular decoding theorem to a decoding problem where the erasures have already been fixed (sampled) suggest that the partitioning into sub-tasks may also be taken to depend on the observed erasures. Constructing the buffer regions in a way which depends on the specific erasure configuration drawn makes intuitive sense. Buffer regions in parts of the protocol with an atypically high proportion of erasures will need to be bigger due to the faster buffer growth through erasure clusters. Conversely, buffer regions with a low proportion of erasure can be kept smaller, possibly reducing to a buffer width of d' for a fragment with no erasures. This suggest a heuristic by which to minimize the size of the needed buffers (or increase the effectiveness of fixed size ones). One should attempt to partition the decoding problem along cuts such that the immediate buffer regions have the smallest density of erasures.

VI. SCHEDULING DECODING TASKS

In this section we define several approaches to modular decoding. In particular, we define a schedule of commit regions and their associated buffers, that determine the set of sub-tasks and their communication requirements. We include a schematic for the system-level data flow requirements of these implementations in App. A.

Logical blocks, ports, and membranes. To specify our schemes, we first need to carefully define the constituents of a surface-code logical space-time network, known as *logical blocks* [9]. A logical block is a set of instructions to implement a logical (i.e., encoded) quantum instrument based on surface codes. These specify the physical instructions that must be implemented to manipulate topological defects of the code, such as primal and dual boundaries [17, 27, 32, 33], transparent domain walls, twists and corners [34–38] in order to realize the desired logical operation. In addition to these topological features, logical-blocks have a set of *ports*, which correspond to the inputs or outputs of the (logical) quantum instrument and carry information encoded using surface-codes. Logical blocks can be composed along ports to build larger logical networks describing fault-tolerant quantum computations.

The connectivity of a logical block network can be described in a simplified way by a directed-acyclic graph (DAG) G_{\log} in which (i) vertices are logical blocks describing a logical quantum instrument and (ii) edges are ports representing a logical quantum system (here, a single logical qubit in a surface code).

The directed edges of G_{\log} define the order in which the logical blocks are performed. In particular, one can label the vertices with integers such that edges point from the vertex with the smallest label to that with the largest. Applying the (logical) quantum instruments sequentially according to this ordering gives a mapping from a collection of logical subsys-

tems to a collection of logical subsystems. As we focus on networks comprised of Clifford quantum instruments, we can describe the network with the stabilizer formalism [9, 16]. In particular, one can define a set of Pauli operators that stabilize each (logical) quantum instrument. Each vertex of the logical block network produces a set of classical outcomes that determines the signs the Pauli operator that stabilize the instrument (i.e., a partial Pauli frame). The specific set of physical outcomes that determine the logical Pauli frame are supported on a logical membranes.

Examples of logical blocks are shown in Fig. 7. We will consider a class of networks where the (logical) quantum instruments are constructed from ZX-networks [30, 39, 40] which we call ZX-instruments following Ref. [16]. Logical blocks realizing these ZX-instruments are shown in Fig. 7. We note that as the instruments are Clifford, we may also change the direction of any edges and have a valid logical block network – as such we often do not draw the arrows explicitly. For a given logical block (or network), we label ports by integers, and use them to index the logical correlators of the network.

The CNOT matrix architecture. To demonstrate the universality of the decoding schemes, we present a universal architecture based on ZX-instruments. The scheme is based on that proposed in Ref. [41]. The architecture can also be understood in the lattice surgery perspective [7], however, this presentation will lead to a logic block network that directly admits a fast modular decoding scheme (as demonstrated in the following subsection).

A universal set of gates on n qubits is given by $\{T_P = \exp(\frac{i\pi}{8}P) \mid P \in \mathcal{P}_n\}$, where \mathcal{P}_n is the n -qubit Pauli group. Similar to a T gate, each gate T_P can be realized by injecting a magic state and applying a generalized CNOT operator before measuring out the auxiliary qubit. The generalized CNOT operator with source Pauli product operator P and target qubit having a Pauli operator X is given by $C_P \text{NOT} = (1 + P + X - PX)/2$. A conditional Clifford correction $S_P = \exp(\frac{i\pi}{4}P)$ must be applied depending on the measurement outcome, as shown in Fig. 7 a). In other words, the generalized CNOT operator, measurements and a supply of magic states is a universal set of operations. Using an additional Y -eigenstate ancilla as a catalyst (that is not consumed) it is possible to implement the generalized CNOT for an arbitrary Pauli operator P using only elementary CNOT operations and two Hadamard operations, as shown in Fig. 7 b). This circuit can be represented as a logic block network with each element being a ZX-instrument as shown in Fig. 7 which we refer to as the CNOT matrix architecture. Each element of the network is a ZX-instrument with a space-time volume of d^3 . See Refs. [9, 16] for more details. This architecture will be used to illustrate the modular decoding schemes.

From logical block networks to scheduling graphs. In the following, we use the graph G_{log} describing the logical block network to determine the scheduling graph G_{sch} , governing the set of sub-decoding problems and their order. We make this choice for convenience and note that one may make other choices of scheduling graphs. For example, nodes of the scheduling graph may be decomposed or coarse grained (just as logical blocks can be) to define alternate decompositions of

the decoding problem. It is desirable for the elementary logical blocks at each vertex to have small volume, such that the processing time for each decoding task is short. The decomposition of fault-tolerant logic into networks of logic block satisfy this desiderata, with each block having a volume of $O(d^3)$.

A. Vertex-only decoding

The first set of schedules we consider, directly obtain the vertices and edges of the scheduling graph from the logical block network. In particular, every logical block (corresponding to a vertex in G_{log}) defines the commit region (corresponding to a vertex in G_{sch}) of a sub-decoding problem, and edges are placed between two blocks whenever they share a port. What remains is to determine the directions \prec of the edges, the order of the decoding sub-tasks which ultimately impacts the reaction time. This is schematically represented in Fig. 8. The buffers for each region can be chosen by considering the neighbouring blocks. One may take all neighbouring blocks connected to the a given block as the buffer, or alternatively use the graph traversal approach described in Sec. IV D to construct the minimum necessary buffers.

Sequential vertex decoding. The simplest schedule is obtained by completely mirroring the logical order in G_{log} in the dependencies and scheduling of decoding tasks making G_{sch} identical to G_{log} . This is called sequential decoding—the sub-tasks proceed in the same order as the logical blocks are performed. If decoder modules can process each decoding block faster than the time it takes a block of input outcome data to be generated by the quantum hardware, this naive approach works fine. In fact, it minimizes reaction time as each block can set the boundary condition for its future neighbours.

However, this approach will generate backlog even if the individual decoder modules take slightly longer to solve decoding tasks than it takes the quantum hardware to produce a block of outcome data. This is true, even if additional decoding power is made available in the form of additional decoder modules. This is a poor parallelization of the global decoding problem and decoder modules will lay idle waiting for other modules to complete their tasks which are needed for input boundary conditions. The data dependency among decoding tasks leads to an accumulating backlog and increasing reaction time with the length of chains in G_{log} .

It is for this reason that it is important to (at least partially) decouple the logical block order of G_{log} and the data dependency order G_{sch} which the decoding of logical blocks should respect. The reason we say *partially decouple* here is because, feed-forward classical control logic in the quantum circuit will need to be respected by both the decoder scheduling G_{sch} as well as consistent with the logical block order. Each logical membrane associated to a logical outcome must be fully decoded before said outcome can be used to condition forthcoming circuit elements. An extreme case of this is presented in Fig. 1, where each T gate implemented via magic state injection leads to a logical outcome which is needed to complete the consumption of the following magic state.

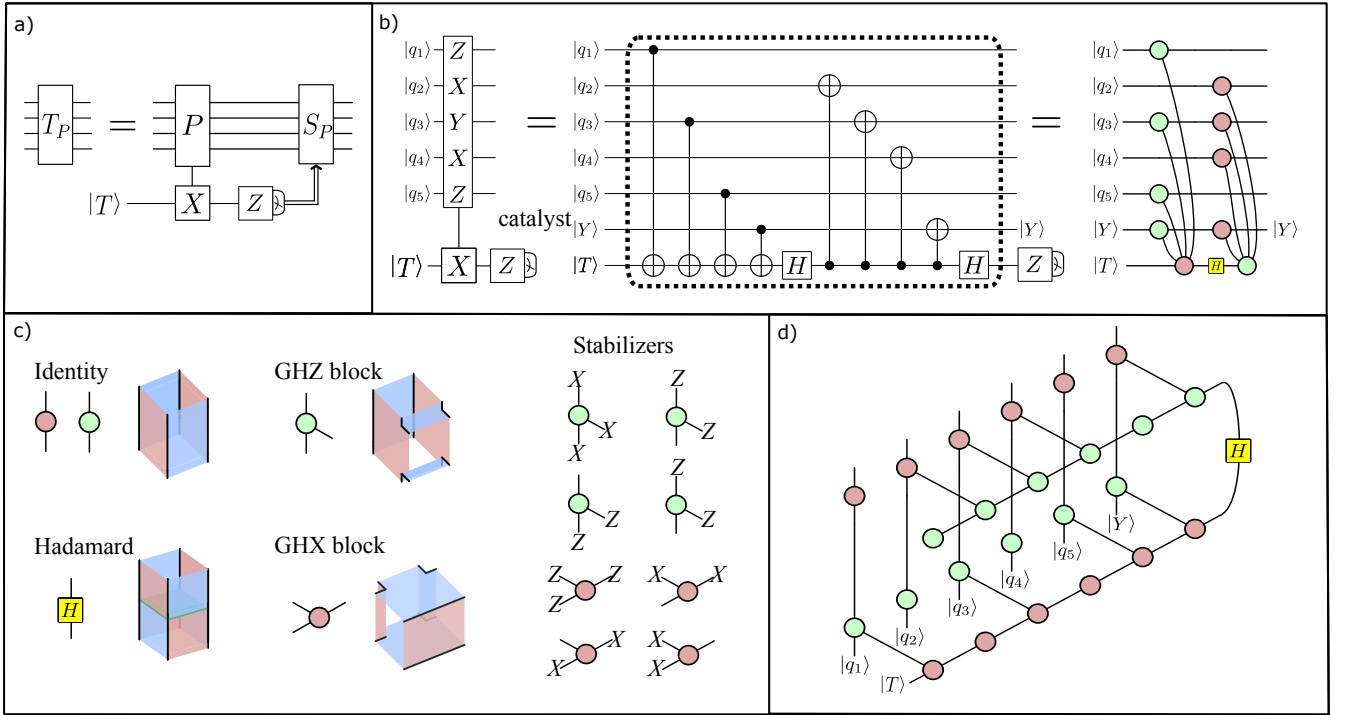


FIG. 7. **(a)** A circuit identity showing how an arbitrary n -qubit $T_P := \exp(i\pi/8P)$ gate, for an n -qubit Pauli product operator P , can be realized by the inclusion of a magic state, along with a generalized CNOT operator controlled on P and conditional $S_P := \exp(i\pi/4P)$ gate conditioned on a single qubit measurement on the injection register. The conditional S_P can be accounted for by the Clifford frame tracking in the fault tolerant setting. **(b)** The generalized CNOT conditioned on P can be realized (dashed box) by a circuit involving sequence of CNOTs, and two Hadamard operators. The decomposition uses a $|Y\rangle$ state (i.e. a Y eigenstate) which is kept unchanged in the process (a catalyst state). The circuit structure can be simplified into a ZX diagram. The figure gives the example of a 5-qubit Pauli operator $P = ZX Y X Z$. **(c)** Each element of the graph G_{\log} is realized by a fault-tolerant logical block. Stabilizers describing the quantum instrument are shown, each one corresponding to a membrane in the logical block. The blue and red boundaries correspond to primal and dual boundaries, following the conventions of Ref. [9]. **(d)** A ZX-diagram equivalent to the one obtained for the 5-qubit example in (b) compatible with elementary logical blocks arranged in a local 3D structure. This is the layout prescribed by the CNOT matrix architecture.

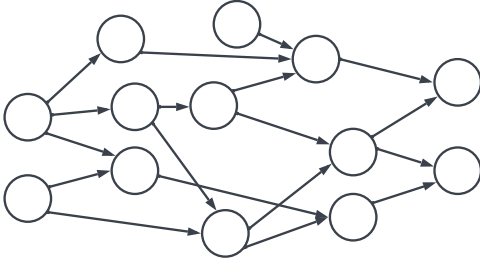


FIG. 8. Directed acyclic graph (DAG) G_{sch} . In our context, each node represents a decoding task $i \in \mathcal{T}$, and each directed edge represents a causal dependence $i \prec j$ imposed whenever the correction κ_i committed by an earlier task affects the syndrome for check generators Σ_j used by a later task. The direction of the edge points from the earlier decoding task to the later one w.r.t. the scheduling.

Parallel vertex decoding. An approach that gives a faster reaction time is to consider a partitioning of the vertices of G_{sch} into a graph coloring, where neighboring vertices have different colors. Indexing the colors by integers

$\{1, 2, \dots, n_c\}$, one can perform all available tasks of the same color in parallel, starting with 1 and proceeding in order. We will still maintain one edge of G_{sch} per edge of G_{\log} , however, their direction will follow increasing color labels. This gives a bound on the reaction time which is proportional to the number of colors (n_c). In particular, if G_{\log} is bi-colorable, we can use this coloring to construct G_{sch} with a very low reaction time, since all causal chains will have depth bounded by 2 (decoding tasks). If sufficiently many decoder modules are available (i.e. decoding throughput is met), this guarantees a reaction time which will not increase with the length of logical dependency chains in G_{\log} as would be the case with sequential decoding. However, each decoding problem while still having volume of order $\mathcal{O}(d^3)$ may still be large, owing to the large combined buffer and commit sizes. We improve on this with *edge-vertex* decoding.

B. Edge-vertex decoding

Here we consider schedules with even lower reaction time than parallel vertex decoding. The approach works by first

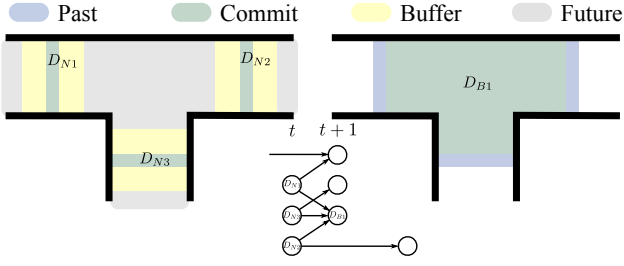


FIG. 9. The figure depicts a four decoding tasks which provide an example of edge - vertex decoding. **(left)** Three edge decoding tasks D_{N1} , D_{N2} , D_{N3} are solved independent of any other decoding task. The outcome data for a significant buffer regions (yellow) must be provided to these tasks in order for them to provide high quality recovery estimates on the commit regions (green). Edge decoding tasks treat unavailable outcomes (grey) as open boundary conditions. Such outcomes may be unavailable, either because they are yet to be produced, or because they are too far from the commit region to be relevant. **(right)** A vertex decoding task is solved (green) with check boundary conditions (blue) imposed by preceding edge decoding tasks. **(bottom center)** The corresponding piece of the scheduling graph G_{sch} , the DAG associated to the decoding tasks presented in the figure. Edge decoding task rely directly on measurement outcomes but not on corrections obtained by any other decoding task. In surface code lattice surgery, each edge decoding task provides boundary conditions to two vertex decoding tasks.

decoding ports between logical blocks, using the neighbouring blocks as buffers. The commit region associated to ports is chosen to be a minimum number of error generator “layers” such that the Tanner graph for the decoding problem becomes disconnected in the direction perpendicular to the port, if the corresponding vertices are removed. This effectively decouples the decoding problem for neighboring blocks. After the ports are committed to, the blocks themselves may be decoded, using no extra buffers as their boundary conditions are now fixed.

Parallel edge-vertex decoding. The scheduling graph G_{sch} is constructed as follows. For each vertex and edge of G_{log} (corresponding to logical blocks and ports, respectively), we place a vertex for G_{sch} . We place a directed edge between a block vertex and any port vertex that belongs to it, directed from the port vertex to the block vertex. Buffers for the port vertices are given by the neighbouring logical blocks. The name of the scheme is derived from the fact that edges of the logical block network are decoded first, followed by the vertices. We give examples of this schedule in the following section. In terms of reaction time, the scheduling graph G_{sch} is bipartite (i.e., depth of 2). This scheme thus has an extremely low reaction time, and as we will numerically be show to performs extremely well in terms of logical error rate.

VII. SIMULATION AND RESULTS

In this section, we first provide a short description of our implementation of the modular decoding scheme for logical block networks, then present extensive simulation results for

Single spider block with three membranes

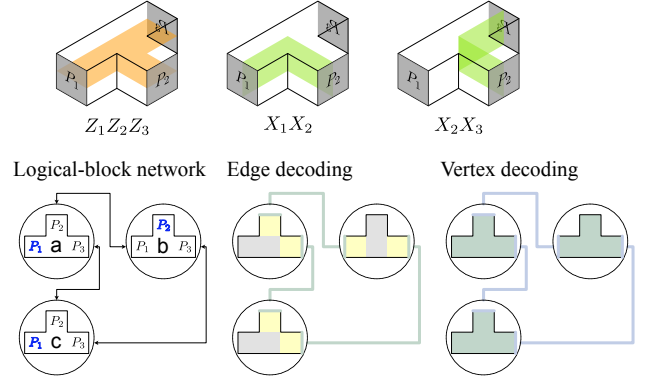


FIG. 10. Schematics of the software implementation of modular decoding. **(top)** An elementary logical block with three ports and three membranes, where each membrane is labeled with the corresponding stabilizer representation. **(bottom left)** A simple logical block network with three vertices $\{a, b, c\}$ and three edges $\{(a, P_2) \leftrightarrow (b, P_1), (a, P_3) \leftrightarrow (c, P_2), (b, P_3) \leftrightarrow (c, P_3)\}$. Here each edge represents an identification of two matching ports from two blocks. Global logical membranes are expressed in terms of stabilizers on the open ports (blue), e.g., there is a global membrane $Z_{a,P_1} Z_{b,P_2} Z_{c,P_1}$, which is the union of all three individual ZZZ -type membranes. **(bottom right)** edge-vertex modular decoding. The interface regions (or *edges* in the logical block network, shown in green) are decoded first in parallel, with buffers growing into bulk regions (yellow). After the edge decoding, remaining disconnected bulk regions (or *vertices* in the logical block network) are decoded in parallel. The edge decoding step sets boundary conditions (blue) for the vertex decoding step.

logical block networks with increasing complexity. We start from a benchmark model of a linear chain of identity blocks. We then move to a planar network of ZX-instruments with a more complicated composition of logical membranes. Finally, we simulate the Clifford part of the 15-to-1 magic state distillation protocol. In each case, we show that with sufficient buffering, the performance of modular decoding approaches that of monolithic decoding.

A. Software implementation

We describe the modular decoder implementation used in our numerical investigation. Firstly, we consider the implementation of the logical block networks. Each elementary logical block defines its own labeled input and output ports. For example, the identity block has an input port and an output port named “IN” and “OUT” respectively. The partial membranes in each logical block are labeled by their stabilizer representations, e.g., the two partial membranes of the identity block are labeled $X_{IN}X_{OUT}$ and $Z_{IN}Z_{OUT}$. Then one can define a logical block network by adding elementary logical blocks as nodes in the network, and specifying the matching of ports among the blocks as edges in the network. The buffer regions (after specifying the buffer size), global membranes, and their specific decomposition into par-

tial membranes are then computed automatically. As an example, we can define a chain of two identity blocks as follows: Add two identity blocks as vertices a and b into the network; add an edge $e = (a, \text{OUT}) \leftrightarrow (b, \text{IN})$. The buffer region will grow (by syndrome-graph traversal) around e until reaching the target buffer size. Global membrane decomposition will be derived, e.g., there will be a global membrane $X_{a,\text{IN}}X_{b,\text{OUT}}$, which is the union of two local membranes represented by $X_{a,\text{IN}}X_{a,\text{OUT}}$ and $X_{b,\text{IN}}X_{b,\text{OUT}}$. This simple design applies to arbitrary logical block networks. See Fig. 10 for schematics for a slightly more complicated example. For the purposes of simulation, any remaining input and output ports of the global problem are treated as a noiseless readout. (See Sec. XII. M. of Ref. [9] for more details on this approach.)

B. Noise model

For the simulations, we assume that the fault-tolerant logical blocks are realised using fusion-based quantum computation with the 6-ring fusion network [9, 12]. Fusions, which are bell basis measurements $\{XX, ZZ\}$ are performed between resource states, which are ring-like cluster states on 6 qubits. Boundaries are realized using certain single qubit measurement patterns. Checks are constructed out of outcomes of fusion measurements: those in the bulk consist of 12 fusion outcomes, while those on the boundary (involving single qubit measurement outcomes) may involve 8 or fewer outcomes. We use the *hardware-agnostic error model* of Ref. [9], where each fusion outcome and single-qubit measurement outcome is subject to an *i.i.d* bit-flip error with probability p_{error} . Under this error model, using the Union-Find decoder, the threshold error rate is $p_{\text{error}}^* = 0.95\%$. We will look at fixing the error rates at $p_{\text{error}} = 0.5\%$, which is approximately half the threshold.

We remark that despite the numerical results being based on fusion-based quantum computation, we expect the qualitative results and conclusions to extend to circuit-based and measurement-based implementations of surface code computations. This is because the decoding problem for all approaches can be expressed in terms of a syndrome-graph, and one may regard the differences as a choice of error model. See secs. VII. and VIII. of Ref. [9] for more details on the scheme and error model.

C. Idling memory

The simplest model for testing modular decoding schemes is in the case of a logical qubit in memory, which can also be thought of as a logical identity block (or chain thereof). The functionality of the full network, in this case a chain of τ identity blocks, is still the identity gate and the two global logical membranes X_0X_τ and Z_0Z_τ are simply concatenations of the two local logical membranes X_tX_{t+1} and Z_tZ_{t+1} for $t \in \{0, \dots, \tau-1\}$. Nevertheless, this setup is enough to show

important aspects of modular decoding, including the need for buffering and optimization of scheduling.

We compare the LER among monolithic decoding (using the union-find decoder), and modular decoding with different buffer sizes (where each modular decoder also utilizes union find). Fig. 11 shows the evolution of LER with increasing buffer sizes, for a variety of protocol fault distances $d = 13, 15, 17, 19$. Without buffering (buffer size $b = 0$), the LER is close to 50%. The LER decreases exponential with initial increase of the buffer size b . However, as the buffer size b approaches the protocol fault distance d , this improvement in LER stagnates. For $b \geq d$, the buffering condition of Def. 2 is satisfied and numerically obtained LER from modular decoding is indistinguishable from monolithic decoding.

D. Planar network of ZX-instruments

In this example, we study a planar network of four logical blocks (see Fig. 12). Each logical block supports partial membranes $Z_1Z_2Z_3Z_4$ and pairwise X_iX_j 's (i.e. a 4GHZ entanglement structure). The logical block network presented has 8 ports, whose partial membranes are $\prod_{i=1}^8 Z_i$ as well as pairwise X_iX_j 's (i.e. a 8GHZ entanglement structure).

In addition to the logical membranes which provide the logical stabilizers for this fragment there is a logical **meta-check**. This meta-check is beyond the scope of the topological fault-tolerance, to which modular decoding is being applied. Meta-checks are the basis for concatenating fault-tolerant protocols and are not included in the group $\langle \Sigma \rangle$ generated by the local check generators Σ . In this example, the meta-check corresponds to a closed membrane composed of four partial XX membranes on the constituent logical blocks but with no support on external ports. In the case of correct topological decoding the "logical" outcome associated to this membrane yields a fixed value. Obtaining a different value is indicative of an error promoted to a logical error by topological decoding, which can nevertheless be caught by the meta-check.

Fig. 12 provides numerical data confirming that the LER from modular decoding approaches that from monolithic decoding quickly with increasing buffer size b .

A key feature of this logical block network is that global membranes come in many different sizes. Note that logical membranes are topological objects, and deformation of a logical membrane by applying (XOR with) parity checks on the syndrome graph simply leads to an equivalent logical membrane. To quantify the size of a logical membrane in a topological way, we count the number of minimal-weight logical errors for the given membrane (i.e., the minimal-weight undetectable errors that intersect the given membrane an odd number of times). This turns out to be a good proxy of LER especially at low physical error rate. We show that the LER is indeed roughly proportional to the size of the logical membrane. Specifically, we collect the LERs from all membranes $\{\text{LER}(\mathcal{M}_i)\}$ and calculate a unit of LER, $p = \sum_i \text{LER}(\mathcal{M}_i) / \sum_i \text{size}(\mathcal{M}_i)$. The membrane-size ansatz reads: $\text{LER}^{\text{ansatz}}(\mathcal{M}_i) = p \times \text{size}(\mathcal{M}_i)$.

The logical decay is useful for quantifying the FT capability

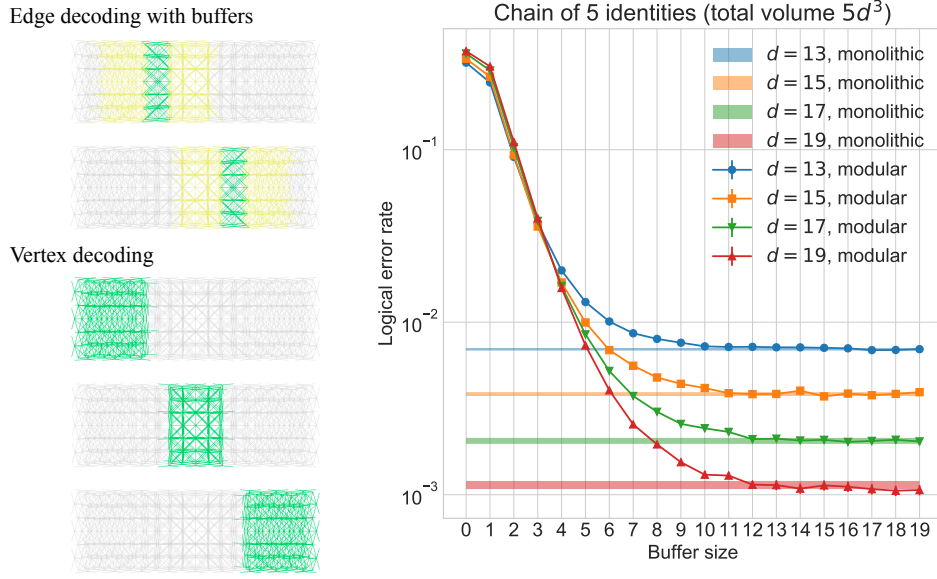


FIG. 11. Modular decoding for a chain of identity blocks. **(left)** Schematics of edge-vertex modular decoding for a chain of 3 identity blocks. In the first edge-decoding step, all interface regions (green) are decoded in parallel with buffers (yellow) grown into neighbouring bulk regions; in the second vertex-decoding step, the bulk regions (green) are decoded in parallel. Here we show the primal syndrome graph, and the LER corresponds to that of the membrane X_0X_5 . Decoding of the dual syndrome graph is similar. **(right)** Impact of buffer size b on modular-decoding logical error rate (LER) for a variety of protocol fault distances d (simulation performed for a chain of 5 identity blocks). Without buffering, the LER is close to 50% per logical membrane; increasing b quickly decreases the LER until it becomes indistinguishable from that of monolithic decoding. Note that in this case the two global logical membranes (X_0X_5 and Z_0Z_5) have the same logical error rate.

of a protocol. It is the speed of the exponential decay of the LER with increasing block size L when the physical error rate is below threshold, i.e., the β obtained when fitting the logical error rate to the relation $\text{LER} = \alpha e^{-\beta L}$ (where α is another fit parameter). A good FT protocol has large β , such that the target LER can be achieved by small L . We observe that with modular decoding, the logical decay increases with buffer size b , approaching to that of monolithic decoding; also, the logical decay on larger membranes are generally smaller than that on smaller membranes.

E. 15-to-1 magic state distillation protocol

The magic state distillation (MSD) protocol is essential for universal quantum computing. We present the first fault-tolerance simulation of the *static*, *Clifford* part of the 15-to-1 MSD protocol. Here *static* means we focus on the MSD protocol before the adaptive measurements of input magic states, and *Clifford* means we ignore errors from the injection of input magic states and focus on errors incurred by the Clifford quantum gates. This part of the 15-to-1 protocol can be realized by a network of logical blocks using the tri-orthogonal matrix representation (which will be explored in an upcoming paper [42]). Specifically, there are 27 logical blocks (16 red ones and 11 green ones), 27 global ports, and 27 global membranes with varying sizes. In the edge-vertex modular decoding scheme, 46 edge-decoding tasks will be performed in parallel first, followed by 27 vertex-decoding tasks.

Fig. 13 shows edge-vertex modular decoding with buffering still performs very well for this fairly large logical block network. In this example, different logical membranes have LERs that are differed by orders of magnitude, because of the drastic difference in the membrane sizes. The LER is still roughly proportional to the membrane size. The logical decay rate β still increases with buffer size, and is in general smaller on larger membranes.

VIII. CONCLUSIONS AND OUTLOOK

We have introduced *modular decoding*, a distributed approach to solving large decoding problems by decomposing them into smaller decoding sub-tasks with minimal data interdependencies. Each sub-task can be solved by a suitable off-the-shelf, offline decoder (such as MWPM [2, 23] or UF[24] for surface-code based schemes) to produce a partial recovery, which are then combined to produce a global correction. Modular decoding is designed to guarantee the availability of logical measurement outcomes as they become necessary for branching decisions throughout the quantum computation. In order to provide these outcomes in a timely manner and avoid slowing down the computation, the decoder must keep up with the continuous stream of measurement data produced. This places stringent requirements on the the decoder subsystem, such as high throughput (keep up with the overall data rate), short reaction times (provide partial results within a short time frame) and minimal LER (logical error rate).

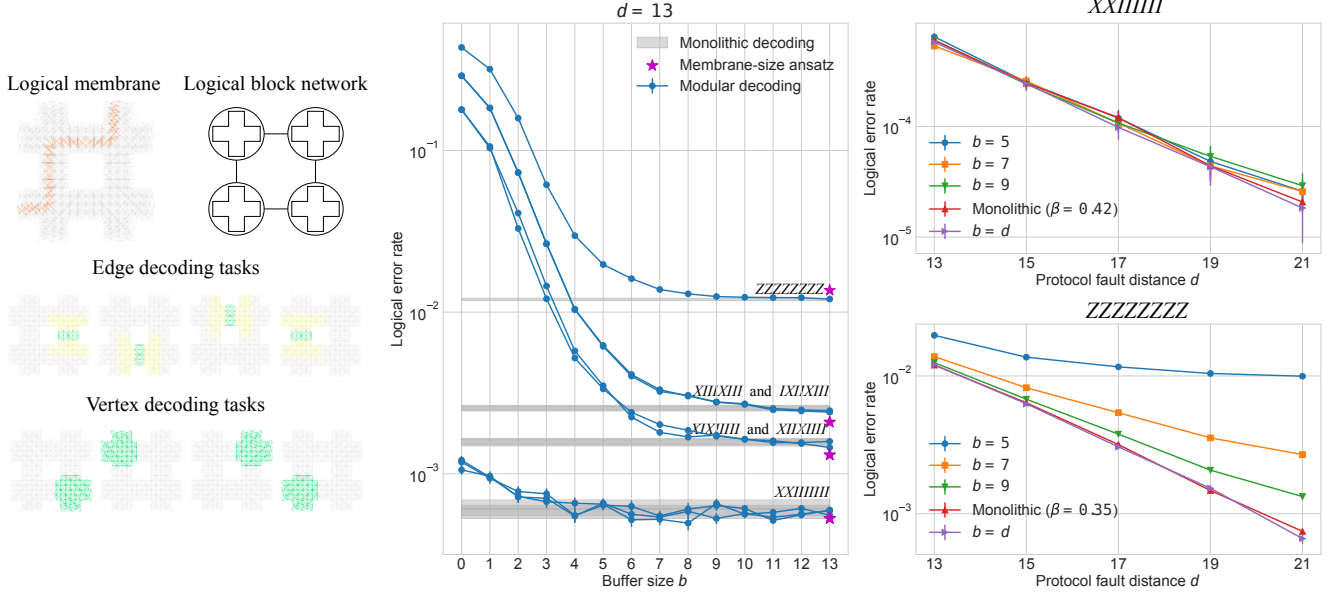


FIG. 12. Edge-vertex decoding on a planar network of logical blocks. **(left)** Logical block network and syndrome graphs for the protocol. The network consists of four 4GHZ logical blocks connected in a ring structure to form an 8GHZ with one meta-check. Orange shading shows one of the logical membranes (corresponding to $IIIXIIIX$ stabilizer), supported on three of the constituent blocks and crossing two port connections. Commit and buffer regions are respectively shaded green and yellow for all decoding tasks (both edge and vertex). **(middle)** Impact of buffer size b on logical error rate (LER) in edge-vertex modular decoding. Each curve corresponds to a different logical membranes in the network and are labeled up to a cyclic shift by 2 and order inversion (i.e. the geometric symmetries of the network). Membranes crossing a larger number of ports have higher LER for low b . For sufficiently large buffer size b , all LERs approach to values from monolithic decoding (shaded horizontal gray lines), which is roughly proportional to membrane size (purple star estimate). **(right)** Logical decay β for selected block and membrane (using stabilizer representation) and buffer sizes b . The $XXIIIIII$ logical membrane is supported on a single logical block and is minimally affected by buffer size (beyond $b \geq 5$). The $ZZZZZZZZ$ logical membrane is supported on all four logical blocks and all four ports. It is maximally sensitive to buffer size b and increasing code distance d does not yield exponential suppression of LER for $d \gg b$.

The main novel features of our decoder, are scalable throughput and low reaction time and these are achieved by design. Scalable throughput is guaranteed by the high degree of parallelism which is achieved by distributing independent decoding tasks to different decoder modules which operate synchronously, as per Fig. 14. Low reaction time (or at least the computational contribution to it) is achieved by making decoding sub-tasks relatively small (i.e. $O(d^3)$ error and check generators, for fault-distance d) and by keeping all data dependence chains in the scheduling graph G_{sch} short. The most extreme example for this is given by what we refer to as *edge-vertex* decoder scheduling which minimizes both task size and data dependence chains and derives its scheduling graph from the connectivity graph G_{log} of the logical block network.

While the main novel features of our approach are essentially guaranteed by construction, most of our work goes into understanding how to retain a competitively low logical error rate (LER) w.r.t. existing decoders. To this end, we provide examples, a rigorous soundness proof (Sec. V) and numerical evidence (Sec. VII). All of these lead us to the same consistent conclusion; In order to retain the original fault-distance of the protocol as well as similarly low LER, it is necessary to supplement each decoding task with a buffer of syndrome in-

formation along a neighborhood of width roughly d (the protocol distance). This is one of the assumed conditions in proving decoder soundness and is found to be necessary and sufficient to achieve an error rate indistinguishable from that of a monolithic decoder with simultaneous access to all syndrome information.

While union find decoder [43] already have an almost linear complexity in the size of the decoding problem input, there are other decoders such as minimum-weight perfect matching [11] or tensor network decoders [44–46] which have a significantly less favorable scaling. While our numerical simulations used a union-find decoder as a base decoder for individual tasks in modular decoding, the soundness proof for modular decoding is completely general. The modular decoding decomposition provided by edge-vertex decoding or other variants guarantee that the computational scaling of the base decoder will only be relevant up to inputs of size $O(d^3)$ beyond which, a linear coarse grained scaling guaranteed by modular decoding kicks in. As such, we expect modular decoding provides a way to *linearize* the coarse grained complexity of arbitrary decoding algorithms without compromising their decoding accuracy. This allows seriously considering other computationally costly decoding algorithms with higher noise thresholds and use them as a base decoders for modular

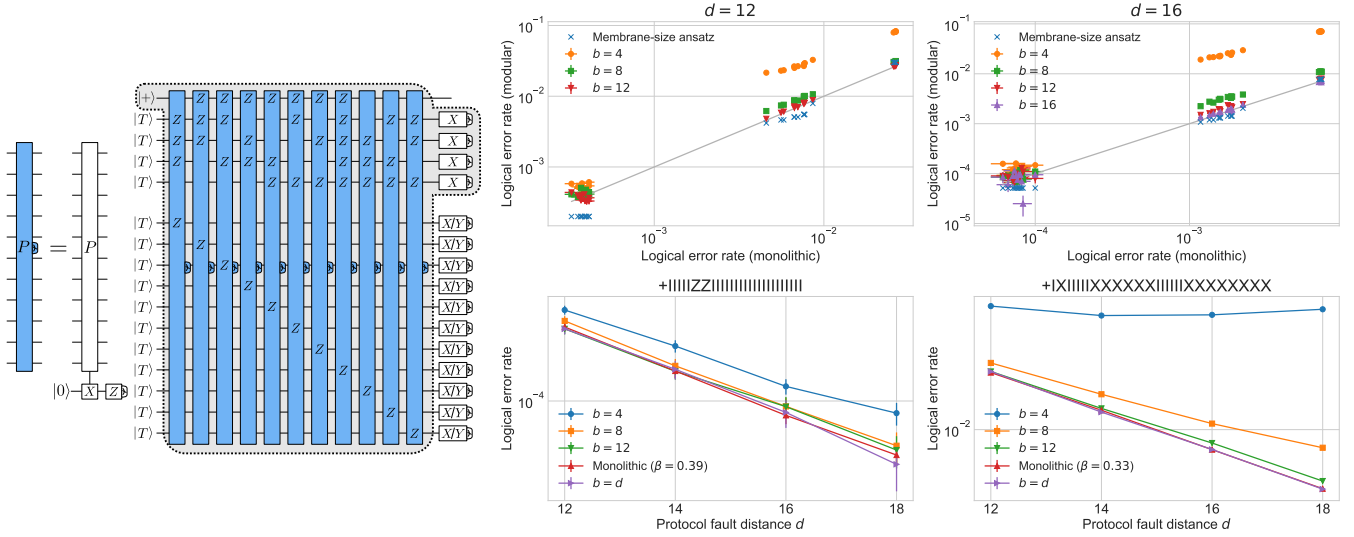


FIG. 13. (left) A blue box notation for non-destructive Pauli measurement of P is introduced to represent the quantum circuit for the 15-to-1 magic state distillation using 11 auto-corrected T gates. The *static Clifford* part is marked with a dashed outline and grey background. The circuit can be reduced to GHZ type logical blocks as in Fig. 7 where modular decoding is performed in two steps. First, parallel edge decoding for all 46 interfaces with buffers, followed by parallel vertex decoding for all the 27 interiors of the GHZ style logical blocks. (right) LER performance of modular decoding on a static Clifford portion of a 15-to-1 magic state distillation protocol. (upper panels) Logical error rate (LER) from modular decoding versus that from monolithic decoding, for the 27 logical membranes (each of the 27 points of a given color represents a logical membrane), and different buffer sizes. With increasing buffering, the performance of modular decoding approaches to monolithic decoding (indicated by the gray $y = x$ line). Larger membranes have larger LERs, and fitting of the LER according to the size of the corresponding logical membrane (blue crosses) agrees well with the actual data. Here the physical error rate is 0.005, which is around half of the fault-tolerance threshold. (lower panels) The left/right panel shows the logical decay for a representative small/larger membrane, which has higher/lower decay constant β , and is less/more sensitive to the buffer size.

decoding.

The methods, and scheduling sections (IV & VI), accurately describe how to decompose a global decoding problem into sub-tasks, schedule these and identify the necessary buffer regions for each task (Sec. IV D) in a way which satisfies all of the desired conditions. Our prescriptions are most concrete for topological quantum circuits (also known as lattice surgery), for which the decomposition into decoding tasks mirrors the graph structure G_{\log} of the logical block network. The simple but powerful buffering method presented (Sec. IV D) is, to our knowledge, a novel contribution. When used with buffer parameter $b = d$ (i.e., the fault-distance of the protocol), the modular decoding scheme obtained is guaranteed to satisfy the decoder soundness. More importantly, the buffering method, is put to the test in combination with edge-vertex decomposition approach and is numerically shown to perform extremely well under the same condition. Moreover, we show the robustness and flexibility of this method by decoding a Clifford circuit fragment of 15-to-1 magic state distillation which is composed of 27 logical blocks with 46 connections among them.

In summary, we have defined modular decoding and shown that it can be instantiated to meet the practical requirements associated with real-time decoding: high throughput, short reaction time and low LER. We look forward to its hardware implementation supporting real-world fault-tolerant quantum computations.

Future directions. While our approach minimizes the impact of the decoding process on the reaction time, in practice, there are further hardware and systems considerations that are relevant. Improvements to the speed of individual decoder units (also known as offline decoders) remain important directions. One can combine our modular approach with the complementary approaches of *pre-decoding* and data compression to further reduce the reaction time. In these approaches, the decoder accuracy is (slightly) sacrificed in order to simplify or speed up the decoding problem [47–49]. The buffer size offers another tunable parameter to trade off reaction-time and logical-error rate performance.

We remark that although we have focused on fault-tolerant schemes based on the surface code, our modular decoding schemes (such as edge-vertex decoding) can readily be applied to any universal computation for fault-tolerant computations based on topological error-correcting codes. For example, our scheme can be applied to color codes in various dimensions [50–54], subsystem color codes [35, 55, 56], and floquet codes [21, 22], and it would be interesting to see if the accuracy is maintained for similar sized buffers. A suitable decoder for sub-tasks will be required in each of these cases. Belief propagation with ordered statistics decoding (BP OSD)—which has shown to have quite good performance for a range of codes [57, 58]—along with renormalization group decoding [59] are examples of suitable decoders.

Beyond topological codes, it may be interesting to ap-

ply modular decoding techniques to the setting of quantum LDPC codes [60–62], or combine them with existing parallel decoders [15]. As quantum LDPC codes with good code-properties require high expansion [63], care is needed to prevent the buffered sub-task from becoming too large.

Finally, it would be interesting to extend the soundness theorem to prove a fault-tolerance threshold theorem for universal computation with surface codes (i.e., a topological analog of the threshold theorem for concatenated codes in Ref. [64]). In particular, one can readily adapt the argument for the lower bounding accuracy threshold in Ref. [2] to include the use of Buffers. In particular, applying this argument to the Clifford part of the CNOT architecture in Fig. 7 can give a lower bound on the fault-tolerant threshold for logical Clifford operations. Taking the minimum of this, and the threshold for distilling magic states [65], one can obtain a threshold theorem for universal computation with surface codes.

IX. CONTRIBUTIONS AND ACKNOWLEDGEMENTS

CD and NN performed the first study in modularizing the decoding problem. CD developed the decoding framework used for numerical simulations. FP and SR performed early research on modular decoding identifying the need for buffering. HB proved soundness of modular decoding under the buffering condition. SR implemented the elementary logical block. YL proposed and implemented the buffer growth algorithm, defined and implemented the logical block networks, implemented the modular decoding simulations and performed the numerical experiments presented in this article. HB has not taken part in the writing of the article or reviewed its final form. YL, FP, SR contributed to writing and reviewing the article as well as figure production. We thank D. Litinski for numerous useful discussions, figures and feedback. We thank all our colleagues at PsiQuantum for helpful discussions and feedback on the draft but especially Terry Rudolph, Dan Dries and Mercedes G. Segovia. FP, YL, and SR would like to dedicate this article to the memory of David Poulin, an inspiring researcher and mentor who left us too soon.

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Appendix A: Modular decoding system-level overview

For a device-level implementation of modular decoding, the classical data from measurements, checks, partial membranes (i.e., decoder output) and logical measurement outcomes need to be relayed to several different processing units. In Fig. 14 we present a system-level schematic for this data flow.

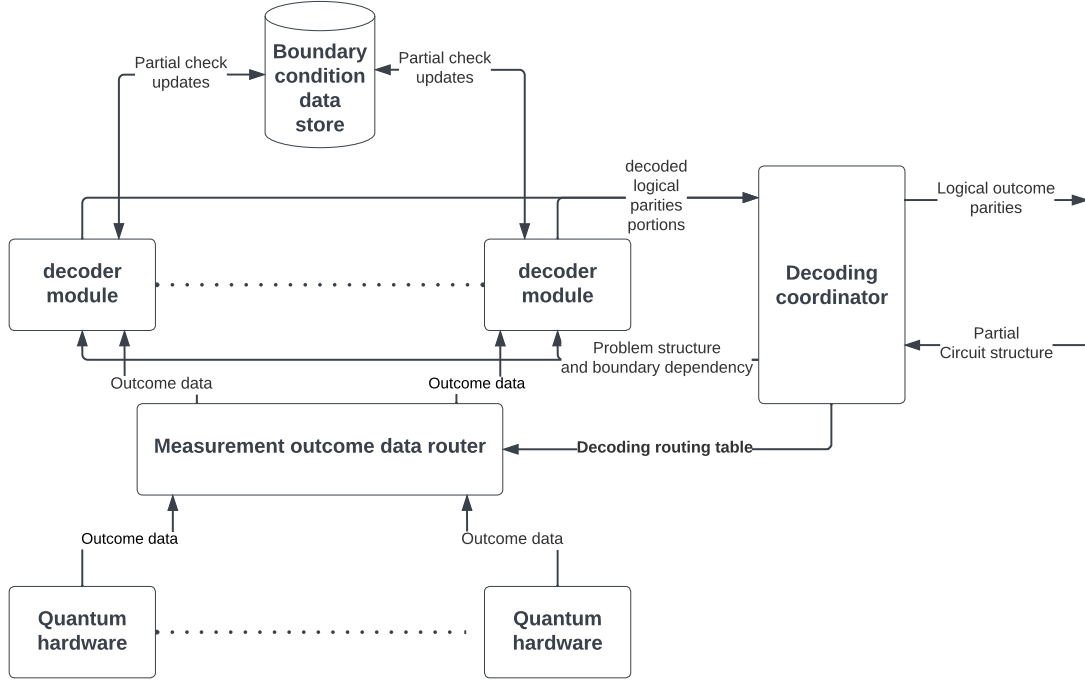


FIG. 14. A schematic for the system-level data flow in a modular decoding implementation. the decoding coordinator has a description of the logical block network, and partitions and schedules the global decoding problem into sub-decoding problems. The decoding coordinator also combines partial membrane outcomes into global membrane outcomes. The quantum hardware units produces a stream of classical outcomes (which may or may not be partially compressed). The measurement outcome data router receives outcome from one or more hardware units and routes it to one or more decoder modules. The decoder modules solve a decoding problem specified by the decoding coordinator. They receive outcome data from the measurement outcome data router as well as any updated checks from the boundary condition data store. After completing their task, they store boundary condition data in the boundary condition data store, and report partial membrane data to the decoding coordinator.