Non-zero crossing current-voltage characteristics of interface-type resistive switching devices

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A number of memristive devices, mainly ReRAMs, have been reported to exhibit a unique non-zero crossing hysteresis attributed to the interplay of resistive and not yet fully understood 'capacitive', and 'inductive' effects. This work exploits a kinetic simulation model based on the stochastic cloud-in-a-cell method to capture these effects. The model, applied to Au/BiFeO₃/Pt/Ti interface-type devices, incorporates vacancy transport and capacitive contributions. The resulting nonlinear response, characterized by hysteresis, is analyzed in detail, providing an in-depth physical understanding of the virtual effects. Capacitive effects are modeled across different layers, revealing their significant role in shaping the non-zero crossing hysteresis behavior. Results from kinetic simulations demonstrate the impact of frequency-dependent impedance on the non-zero crossing phenomenon. This model provides insights into the effects of various device material properties, such as Schottky barrier height, device area and oxide layer on the non-zero crossing point.

The transition from standard CMOS-based devices to memristive devices is a revolutionary advancement in electronics and computing. For decades, the electronics industry has been dominated by CMOS-based devices. However, memristive devices have emerged as a promising alternative with distinctive attributes¹. Memristive devices can retain information about the amount of charge that flows through them, as demonstrated in their history-dependent resistance function^{2–4}. As charge accumulates, the conductance of the memristor can change and remain altered until a charge reset occurs. One of the main fingerprints of all memristive devices is their pinched current-voltage characteristics (*I-V* curves) or hysteresis⁵.

The *I-V* curves of memristive devices typically exhibit a pinched hysteresis shape, arising from their nonlinear dynamics. Notably, there is a zero crossing point where current becomes zero at zero voltage⁵. However, several 'real-world' devices, mainly resistive switching random access (ReRAM) devices, have shown a non-zero crossing hysteresis, indicating presence of some charge, like in a battery^{7–11}. Literature suggests that capacitive and virtual inductive effects contribute to this phenomenon. It is important to note that at least the later effects are not due to physical inductances but could be due to different processes that contribute to switching. This means that it would be more appropriate, as mentioned by Qingjiang et al.¹² to consider the nonlinear change in resistive switching

as a change in the impedance rather than just memristance. Such a nonlinear interplay of resistive, capacitive, and virtual inductive effects introduces frequency-dependent impedance, affecting the phase relationship between voltage and current and generating higher harmonics.

Modeling and simulation techniques provide powerful tools for understanding the impact of capacitive and virtual inductive effects on non-zero crossing hysteresis in I-V curves of memristive devices. Including ion/vacancy transport and capacitive effects in memristive device models is essential, with inductive effects included as inertia effects in particle transport, as explained later. Consequently, we will use the term 'inertia effects' rather than 'inductive effects'. Several proposed models simulate particle transportbased resistive devices in ReRAMs, offering multidimensional computational¹³⁻¹⁶ and compact models suitable for circuit simulations^{17–19}. Compact models for filamentary devices, including capacitive and/or inductive effects, are published^{12,20,21}, such models for interface-type ReRAMs are currently unavailable. Existing models also don't fully account for physical and chemical processes contributing to stochastic vacancy transport and virtual effects.

This paper examines the nonlinear behavior of interfacetype memristive devices, utilizing a kinetic simulation model based on the stochastic cloud-in-a-cell (CIC) method for the bismuth ferrite oxide memristive device (BFO)⁶. Unlike the state-of-the-art compact models, this method more precisely incorporates the stochastic ion or vacancy transport (like the multidimensional computational models), whereas it is fast and accurate like the state-of-the-art compact models. In this paper, the CIC model proposed by Yarragolla et al.^{6,22,23} mainly for interface-type ReRAMs is further modified to incorporate capacitive and inertia effects.

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FIG. 1. (a) The modified equivalent circuits of BFO device⁶ with parallel capacitors across different layers. (b) Different capacitive components in BFO. (c) Depletion layer width variation at LRS and HRS

Typically, the interface-type memristive devices are two-terminal ReRAM devices consisting of a three-layer metal-insulator-metal stack with either a Schottky or tunneling contacts at the metal/oxide interfaces and a solid-state electrolyte sandwiched between these interfaces. The resistive switching in these devices takes place by the drift-diffusion or trapping-de-trapping of charged defects, i.e., positively charged oxygen vacancies in Au/BiFeO₃/Pt/Ti BFO device⁹. The simulation and modeling of such a mechanism have already been demonstrated for BFO using the CIC method. For a detailed description of the method, refer to the work by Yarragolla et al.^{6,22} The pseudo-code of the method and the device-specific parameters used in this work are provided in the supplementary material.

Vacancy transport: In the CIC-based approach, the solution of particle transport and the electric field are conducted iteratively. For an input voltage bias, the particles are transported based on their drift velocity, calculated using the activation energy, U_A , and electric field, E, obtained by solving the Poisson equation. The drift velocity is calculated as follows based on the probability of the particle movement from one lattice site to another^{24,25},

$$v_{\rm D} = v_0 d \, \exp\left(-\frac{U_{\rm A}}{k_{\rm B}T}\right) \sinh\left(\frac{|z| \, e dE}{k_{\rm B}T}\right),\tag{1}$$

where *d* is the lattice constant, v_0 is the phonon frequency, k_B is the Boltzmann constant, *e* is the elementary charge, *T* is the temperature, and *z* is the charge number of the ion. Once the ion or vacancy transport is completed, the electrical parameters, such as the currents and voltages across different layers, are calculated. To incorporate capacitive effects, parallel capacitors are added across different layers in the equivalent circuit models of BFO, as illustrated in Fig. 1(a). The modified equivalent circuit yields the following equations by applying

Kirchhoff's current and voltage laws:

$$I_{SC_t} + I_{C,SC_t} = I_{BFO} + I_{C,BFO} = -(I_{SC_b} + I_{C,SC_b}) = I$$
, and (2)

$$V_{\text{Device}} = V_{\text{SC}_{\text{t}}} + V_{\text{BFO}} - V_{\text{SC}_{\text{b}}}.$$
(3)

For simplicity, we assume an equal voltage drop across the Schottky contact or oxide, and the capacitors. The resistive current through the Schottky contact is computed as follows²⁶,

$$I_{\rm SC} = A_d A^* T^2 \exp\left\{\frac{-\Phi_{\rm SC}}{k_B T}\right\} \left(\exp\left\{\frac{eV_{\rm SC}}{n_{\rm SC} k_B T}\right\} - 1\right). \quad (4)$$

Here n_{SC} is the ideality factor, Φ_{SC} is the Schottky barrier height, and A^* is the effective Richardson constant. Moreover, the current across the oxide region is given by the general Ohm's law,

$$I_{\rm BFO} = \sigma_{\rm BFO} A_{\rm d} \frac{V_{\rm BFO}}{l_{\rm BFO}},\tag{5}$$

where $l_{\rm BFO}$ is the length of the active BFO oxide layer and σ is its conductivity of BFO.

Capacitive effects: Identifying and characterizing capacitive elements in nanoscale devices requires an in-depth exploration of the intricate processes within these structures. At this scale, ReRAM devices demonstrate complex behaviors influenced by factors like metal-insulator interfaces, vacancy transport, and interlayer interactions. Capacitive elements within the device can be distinguished based on specific functions in different regions, including charge storage at metal-oxide interfaces, capacitance related to defects and interfaces, dielectric layer capacitance, and interlayer capacitance in multilayered structures. To determine capacitive components in interface-type devices, Mohamed et al.'s²⁰ approach for filamentary devices is followed, as shown in Fig. 1(b). This



FIG. 2. The change in (a) input voltage, (b) capacitance, (c) depletion layer width, and (d) capacitive current across the top and bottom Schottky contact.

includes capacitance between the interface and defects, capacitance between positive and negative defects, oxide capacitance, and capacitance at the interfaces. Capacitive effects are modeled using effective capacitance values, and the methods for modeling capacitance across these interfaces are discussed below.

The capacitance of a Schottky contact is affected by the dynamics of the depletion layer, a region near the interface of metal and semiconductors with a lack of charge carriers. Changes in the depletion layer's width occur as charge accumulates or depletes in this region, ultimately affecting the overall capacitance of the Schottky contact²⁷. This is demonstrated in Fig. 1c. When a positive voltage is applied to the metal-semiconductor junction, the barrier height decreases, attracting more charge carriers to the interface and causing a narrowing of the depletion layer. Some electrons may flow through the barrier toward the metal electrode, leaving positively charged empty traps near the interface. In contrast, applying a negative bias raises the barrier and prevents electrons from flowing through it. Yet they may be injected into the empty traps. This causes the traps to become neutral and resume functioning, increasing the depletion width²⁸. The change in depletion layer width corresponds to fluctuations in the capacitance of the Schottky contact. The depletion region width can be determined based on the charge accumulation of the effective barrier height at the metal/oxide interfaces as follows:

$$d_{\rm SC} = \sqrt{\frac{2\varepsilon_0 \varepsilon_{\rm r,BFO} \left(\Phi_{\rm SC} - qV_{\rm SC} - k_{\rm B}T\right)}{en}},\tag{6}$$

$$d_{\rm SC_{eff}} = d_{\rm SC}(1 + \lambda_d q(t)), \tag{7}$$

where ε_0 is the vacuum permittivity, $\varepsilon_{r,BFO}$ is the relative permittivity of BFO and n is the defect density. Eq. (7) de-



FIG. 3. The experimental and simulated I-V curves of BFO memristive devices with and without the capacitive effects (C).

fines the rate at which the depletion layer width changes where λ_d is the fitting parameter between 0 and 1, chosen to match the simulation results with experiments and q(t) = $\frac{d_{\rm BFO}(t) - d_{\rm BFO,initial}}{\bar{\tau}}$ is the internal state of the device, where ial

$$d_{\rm BFO} = \frac{\sum_{i=1}^{N_{\rm vacancies}} \left(\bar{x}_{\rm i} - \bar{x}_{\rm SC_b}\right)}{N_{\rm vacancies}}.$$
(8)

Here, \bar{x}_i is the position of i^{th} mobile vacancy, \bar{x}_{SC_b} is the position of bottom Schottky contact and Nvacancies is the number of mobile vacancies.

The capacitance of the Schottky junction can be determined by utilizing the electrostatic capacitance equation applied in a parallel plate capacitor using the permittivity of the oxide layer. Furthermore, the general electrostatic capacitance equation is employed to determine the capacitance across a solid-state electrolyte. Here, the effective capacitance resulting from the capacitance between different charged defects and defects and interface is considered.

The electrostatic capacitance and the current can be calculated using the following formula respectively:

$$C_{\rm SC/BFO} = \frac{\varepsilon_0 \varepsilon_{\rm r, BFO} A_{\rm d} r_{\rm C}}{d_{\rm SC_{\rm eff}/BFO}} \text{ and } (9)$$

$$I_{\rm C,SC/BFO} = C_{\rm SC/BFO} \frac{\mathrm{d}V_{\rm SC/BFO}}{\mathrm{d}t} \tag{10}$$

Capacitance is often adjusted by a roughness factor, reflecting deviation of the actual surface area from the ideal geometric area. Similarly, here, a correction factor ($r_{\rm C} \in (0,1)$) aligns simulations with experiments, addressing nanoscale non-idealities. $r_{\rm C}$ represents capacitance reduction and considers factors like dielectric heterogeneity, interface effects, frequency dependence, oxide thickness variations, quantum effects, and process-related variability. Through iterations, an optimal value of $r_{\rm C}$ minimizes disparities between theoretical predictions and experimental results under diverse conditions.



FIG. 4. (a)-(d) The shift in non-zero crossing point, (e)-(h) the change in q(t) and (i)-(j) the change in bottom Schottky contact capacitance of the device due to the bottom Schottky contact barrier ((a),(e),(i)), BFO permittivity ((b),(f),(j)), BFO layer length ((c),(g),(k)), and the area of the device ((d),(h),(l)). The different colored points in plots (a)-(d) indicate the voltage and current at the non-zero crossing point.

The depletion layer width, its corresponding capacitance, and current across Schottky contact capacitors are displayed in Fig. 2 for the BFO device. For an input voltage given in Fig. 2(a), the top depletion layer width (d_{SC_t}) near the Au electrode slightly increases while the bottom depletion layer width (d_{SC_b}) near the Pt electrode decreases as shown in Fig. 2(c). As oxygen vacancies move towards the Pt electrode, the changes in the top and bottom Schottky barrier heights result in this phenomenon. The capacitance plot (Fig. 2(b)) and capacitive current plot (Fig. 2(d)) reveal that the capacitance across the bottom Schottky contact has a significant impact on the overall capacitive effects in BFO.

Inertia effects: The equation that controls the movement of charged particles considering drift velocity and friction, mimics the language of an electrical circuit. This model displays the system as a group of interconnected resistors and inductors, linking particle dynamics with circuit characteristics. This perspective is based on a fundamental approach, i.e., a simplified momentum conservation equation for positive charge carriers,

$$m\frac{\mathrm{d}v_{\mathrm{D}}}{\mathrm{d}t} = eE - m\gamma v_{\mathrm{D}} \tag{11}$$

Here, v_D is the drift velocity, *E* is the driving electric field, γ is the frequency for collisions of charged particles with the atoms of the background lattice. *m* and *e* are the particle mass and charge, respectively. After multiplying the momentum equation with *e* and the particle density *n* and defining the current density by $j = env_D$, we get a so-called generalized Ohm's law

$$\frac{\mathrm{d}j}{\mathrm{d}t} = \frac{e^2 n}{m} E - \gamma j \tag{12}$$

In principle, this is nothing but the Drude model of electrical conduction in materials (especially metals). Assuming a homogeneous one-dimensional scenario, we can introduce the current by $I = jA_d$ and the voltage by $V = E l_{BFO}$. Substituting this, we find

$$\mathcal{V}_{\rm BFO} = \frac{ml_{\rm BFO}}{e^2 n A_{\rm d}} \frac{dI_{\rm BFO}}{dt} + \frac{ml_{\rm BFO}}{e^2 n A_{\rm d}} \gamma I_{\rm BFO} = L_{\rm BFO} \frac{dI_{\rm BFO}}{dt} + R_{\rm BFO} I_{\rm BFO}$$
(13)

In this context, $R_{\rm BFO}$ represents ohmic resistance, and $L_{\rm BFO}$ represents an inductance of oxide layer. However, it is important to note that $L_{\rm BFO}$ does not refer to electromagnetic induction. Instead, it serves as a model for inertial effects due



FIG. 5. The simulated *I-V* curves obtained for a sinusoidal input voltage with various frequencies and amplitudes of (a) 4.5 V, (b) 6.5 V, (c) 8.5 V and (d) 10.5 V. Dotted lines in each plot indicate the non-zero crossing points.

to the finite mass of the charged particles involved.

When modeling ion motion in an oxide, it is crucial to allow for the impact of inertia. The momentum equation (generalized Ohm's law) accurately calculates the average velocity of charged particles, comprising ions and electrons, experiencing an electric field. Consequently, the equation for the voltage drop mirrors the charged particles' movement due to an electric field. It, therefore, includes resistive and inertia effects, and integrating these effects eliminates the need for a separate evaluation when explaining the intricate vacancy movement in an oxide.

By incorporating the above-discussed Eqs. (6)-(13) into the CIC model for different layers of BFO, the I-V curves shown in Fig. 3 are obtained that illustrate the nonlinear behavior of BFO devices resulting from the coexistence of resistive, capacitive, and inertia effects. To obtain the I-V curves shown in Fig. 3, an input voltage (Fig. 2(a)) of 8.5 V was utilized, in conjunction with the parameters used by Yarragolla et al.⁶ in Table S1. The figure compares the I-V curves of BFO with and without capacitive effects. A non-zero crossing at -0.21 V is observed for the red curve, even without capacitive effects. Via simulations, we observed that this crossing is random, i.e., we may observe a zero crossing or a non-zero crossing, and it varies between different voltage cycles and devices due to unpredictable stochastic vacancy movement influenced by the electric field and activation energy. Rapid vacancy motion during reset linked to the two-order magnitude increase in vacancy mobility during negative bias, as reported by Du et al.⁹, causes a non-zero crossing in some cycles, highlighting

the stochastic nature of vacancy dynamics. As mentioned by Qingjiang et al., inductive effects can also contribute to nonzero crossing¹²; based on this, we attribute this vacancy motion during RESET to changes in virtual inductivity, which we refer to in this paper as inertial effects. Furthermore, including capacitive effects, the resulting curve (blue) has a similar nonlinear current variation with the input voltage. It reveals similar hysteresis characteristics but with a noticeable non-zero crossing. This curve highlights a precisely similar change in current with the crossing point shifted to -2.9 V, as observed in the experimental *I-V* curve (black).

Analyzing the shifts of non-zero crossing points in BFO device I-V curves under various parameters provides insights into the interplay of capacitive and inertia effects. These simulation-based findings offer a better understanding of device-switching behavior in response to changes in device parameters, a perspective that may not be easily studied experimentally. An isolated variation of the different capacitive components supports the attribution of the underlying mechanism. As shown in Fig. 4(a), the capacitance should decrease with higher barrier height, shifting to lower voltages. However, the observed shift in the crossing point to higher V_{Device} is more significant, attributed to changes in inertia effects. The alterations in the BFO device parameters can affect the electric potential and electric field, affecting vacancies' mobility and drift velocity. This change in drift velocity indirectly affects the inertia effects discussed earlier in Eqs. (11)-(13). Consequently, the position of the vacancies and, therefore, q(t) is also altered, which can be considered a way of measuring inertia effects. As illustrated in Fig. 4(e)-(h) and Fig. 4(i)-(l), monitoring q(t) and capacitance, respectively, can illuminate these dynamics for a comprehensive understanding. For similar reasons, changes in BFO oxide permittivity shift the crossing point to lower voltages (Fig. 4(b)) with increased capacitance, but the influence on device operation remains almost constant. Furthermore, variations in BFO layer length as shown in Fig. 4(c) result in a shift to lower voltages due to the inverse relationship between depletion layer width and capacitance. This shift is primarily due to the interplay of capacitive and inertia effects. Lastly, modifications in the device area lead to a vertical upward shift in currents, as increased capacitance is outweighed by resistive current dominance (Fig. 4(d)). In summary, the mechanism of non-zero crossing in the overall switching kinetics in ReRAM devices is a complex phenomenon involving resistive, capacitive, and inertia effects (unrelated to any induction). To further support this, we included the corresponding *I-V* curves in Fig. S1 and plotted the terms in Eq. (13) to demonstrate the inertia effects in Fig. S2 of the supporting material.

The frequency-dependent behavior of memristive devices requires a comprehensive exploration due to the notable alterations induced by the introduction of capacitive and inertia effects on their nonlinearity and non-zero crossing hysteresis. Fig. 5 shows different *I-V* curves for a BFO device under sinusoidal input voltages with different amplitudes and frequencies. The plots reveal several observations. Increasing the maximum device voltage ($V_{\text{Device,max}}$) at a constant frequency amplifies the hysteresis lobe region, correlating with oxygen

vacancy repositioning in the BFO^{18,22}. Higher voltages exert stronger forces on vacancies, causing them to drift toward the Pt interface, which alters the q(t) and hence the impedance. This phenomenon is more prevalent at lower frequencies.

At higher frequencies, the hysteresis loop area decreases, limited by the time for lattice jumps and affecting resistive switching. Beyond 10 Hz, the I-V curves exhibit resistor-like behavior in BFO. This can be explained by the dynamic interplay of capacitive and resistive effects at varying frequencies, leading to hysteresis saturation. At increased (decreased) frequencies, the capacitive reactance $(X_{\rm C} = 1/2\pi fC)$ rapidly decreases (increases), leading to a swift rise (fall) in capacitive current. Finally, the capacitive effects, identified as the 'battery effect', significantly impact the zero-crossing current. The crossing points deviate from the origin more frequently as the voltage increases¹². As capacitance increases with frequency, resulting in reduced capacitive reactance and enhanced charge storage, the system's battery effect intensifies, shifting the crossing point away and leading to a nearly linear current change at 100 Hz, thereby eliminating the nonzero crossing. Only the parameters for the bottom Schottky contact are plotted in Fig. 4 and Fig. 5 due to their significant influence on the device's switching behavior over the top Schottky contact and oxide layer.

Simulated results confirm capacitive and inertia effects contribute to non-zero crossing hysteresis in the BFO device, particularly noticeable at higher frequencies, adding complexity to its switching characteristics. The research proposes a robust model to comprehend inherent nonlinearity in interfacetype ReRAM devices, facilitating frequency response analysis. Incorporating these effects into simulation models for all ReRAM devices is crucial beyond BFO. Understanding derived from such models is vital for advancing research and optimizing ReRAMs for applications in neuromorphic computing and hardware security. The model captures the complex interplay of resistive, capacitive, and inertia effects, providing valuable insights for maximizing ReRAM potential in emerging technologies.

AUTHOR CONTRIBUTIONS

S. Yarragolla: Methodology, Software, writing – original draft; T. Hemke: Software, Writing – review & editing; J. Trieschmann: Supervision, Writing – review & editing; T. Mussenbrock: Methodology, Supervision, Writing – review & editing.

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DATA AVAILABILITY STATEMENT

Data available on request from the authors.

- ¹M.-K. Song, J.-H. Kang, X. Zhang, W. Ji, A. Ascoli, I. Messaris, A. S. Demirkol, B. Dong, S. Aggarwal, W. Wan, S.-M. Hong, S. G. Cardwell, I. Boybat, J.-s. Seo, J.-S. Lee, M. Lanza, H. Yeon, M. Onen, J. Li, B. Yildiz, J. A. del Alamo, S. Kim, S. Choi, G. Milano, C. Ricciardi, L. Alff, Y. Chai, Z. Wang, H. Bhaskaran, M. C. Hersam, D. Strukov, H.-S. P. Wong, I. Valov, B. Gao, H. Wu, R. Tetzlaff, A. Sebastian, W. Lu, L. Chua, J. J. Yang, and J. Kim, "Recent advances and future prospects for memristive materials, devices, and systems," ACS Nano **17**, 11994–12039 (2023), pMID: 37382380, https://doi.org/10.1021/acsnano.3c03505.
- ²L. Chua, "Resistance switching memories are memristors," Applied Physics A **102**, 765–783 (2011).
- ³D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," Nature 453, 80–83 (2008).
- ⁴D. Ielmini and R. Waser, *Resistive Switching: From Fundamentals of Nanoionic Redox Processes to Memristive Device Applications* (John Wiley & Sons, Ltd, 2016).
- ⁵L. Chua, "If it's pinched it's a memristor," Semiconductor Science and Technology **29**, 104001 (2014).
- ⁶S. Yarragolla, N. Du, T. Hemke, X. Zhao, Z. Chen, I. Polian, and T. Mussenbrock, "Physics inspired compact modelling of bifeo3 based memristors," Scientific Reports **12**, 20490 (2022).
- ⁷B. Sun, Y. Chen, M. Xiao, G. Zhou, S. Ranjan, W. Hou, X. Zhu, Y. Zhao, S. A. Redfern, and Y. N. Zhou, "A unified capacitivecoupled memristive model for the nonpinched current-voltage hysteresis loop," Nano Letters **19**, 6461–6465 (2019), pMID: 31434487, https://doi.org/10.1021/acs.nanolett.9b02683.
- ⁸I. Salaoru, Q. Li, A. Khiat, and T. Prodromakis, "Coexistence of memory resistance and memory capacitance in tio2 solid-state devices," Nanoscale Research Letters **9**, 552 (2014).
- ⁹N. Du, N. Manjunath, Y. Li, S. Menzel, E. Linn, R. Waser, T. You, D. Bürger, I. Skorupa, D. Walczyk, C. Walczyk, O. G. Schmidt, and H. Schmidt, "Field-driven hopping transport of oxygen vacancies in memristive oxide switches with interface-mediated resistive switching," Phys. Rev. Applied **10**, 054025 (2018).
- ¹⁰Y. Xu, L. Tan, B. Sun, M. Lei, Y. Zhao, T. Li, L. Zheng, S. Zhu, Y. Zhang, and Y. Zhao, "Memristive effect with non-zero-crossing current-voltage hysteresis behavior based on ag doped lophatherum gracile brongn," Current Applied Physics **20**, 545–549 (2020).
- ¹¹C. Yang, B. Sun, G. Zhou, H. Zhao, S. Zhu, C. Ke, Y. Zhao, and H. Wang, "Evolution between volatile and nonvolatile resistive switching behaviors in ag/tiox/ceoy/f-doped sno2 nanostructure-based memristor devices for information processing applications," ACS Applied Nano Materials 6, 8857– 8867 (2023), https://doi.org/10.1021/acsanm.3c01282.
- ¹²L. Qingjiang, A. Khiat, I. Salaoru, C. Papavassiliou, X. Hui, and T. Prodromakis, "Memory impedance in tio2 based metal-insulator-metal devices," Scientific Reports 4, 4522 (2014).
- ¹³S. Dirkmann, M. Hansen, M. Ziegler, H. Kohlstedt, and T. Mussenbrock, "The role of ion transport phenomena in memristive double barrier devices," Scientific Reports 6, 35686 (2016).
- ¹⁴S. Dirkmann, J. Kaiser, C. Wenger, and T. Mussenbrock, "Filament Growth and Resistive Switching in Hafnium Oxide Memristive Devices," ACS Applied Materials and Interfaces **10**, 14857–14868 (2018).
- ¹⁵C. Funck and S. Menzel, "Comprehensive model of electron conduction in oxide-based memristive devices," ACS Applied Electronic Materials 3, 3674–3692 (2021), https://doi.org/10.1021/acsaelm.1c00398.
- ¹⁶J. Aeschlimann, F. Ducry, C. Weilenmann, J. Leuthold, A. Emboras, and M. Luisier, "Multiscale modeling of metal-oxide-metal conductive bridging random-access memory cells: From ab initio to finite-element calculations," Phys. Rev. Appl. **19**, 024058 (2023).

- ¹⁷Z. Jiang, Y. Wu, S. Yu, L. Yang, K. Song, Z. Karim, and H.-S. P. Wong, "A compact model for metal–oxide resistive random access memory with experiment verification," IEEE Transactions on Electron Devices **63**, 1884– 1892 (2016).
- ¹⁸M. Maestro-Izquierdo, M. B. Gonzalez, F. Campabadal, J. Suñé, and E. Miranda, "A new perspective towards the understanding of the frequencydependent behavior of memristive devices," IEEE Electron Device Letters 42, 565–568 (2021).
- ¹⁹C. Bengel, A. Siemon, F. Cüppers, S. Hoffmann-Eifert, A. Hardtdegen, M. von Witzleben, L. Hellmich, R. Waser, and S. Menzel, "Variabilityaware modeling of filamentary oxide-based bipolar resistive switching cells using spice level compact models," IEEE Transactions on Circuits and Systems I: Regular Papers 67, 4618–4630 (2020).
- ²⁰M. G. A. Mohamed, H. Kim, and T.-W. Cho, "Modeling of memristive and memcapacitive behaviors in metal-oxide junctions," ScientificWorldJournal **2015**, 910126 (2015).
- ²¹M. Berruet, J. C. Pérez-Martínez, B. Romero, C. Gonzales, A. M. Al-Mayouf, A. Guerrero, and J. Bisquert, "Physical model for the current–voltage hysteresis and impedance of halide perovskite memristors," ACS Energy Letters 7, 1214–1222 (2022), https://doi.org/10.1021/acsenergylett.2c00121.

- ²²S. Yarragolla, T. Hemke, J. Trieschmann, F. Zahari, H. Kohlstedt, and T. Mussenbrock, "Stochastic behavior of an interface-based memristive device," Journal of Applied Physics **131**, 134304 (2022).
- ²³S. Yarragolla, T. Hemke, and T. Mussenbrock, "A generic compact and stochastic model for non-filamentary analog resistive switching devices," in 2023 12th International Conference on Modern Circuits and Systems Technologies (MOCAST) (2023) pp. 1–4.
- ²⁴P. G. Bruce, *Solid State Electrochemistry*, Chemistry of Solid State Materials (Cambridge University Press, 1994) Chap. 3.
- ²⁵R. Meyer, L. Schloss, J. Brewer, R. Lambertson, W. Kinney, J. Sanchez, and D. Rinerson, "Oxide dual-layer memory element for scalable nonvolatile cross-point memory technology," in *Proceedings - 9th Annual Non-Volatile Memory Technology Symposium, NVMTS* (2008).
- ²⁶S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices* (John Wiley & Sons Ltd., 2007).
- ²⁷M. Grundmann, *The Physics of Semiconductors: An Introduction Including Nanophysics and Applications*, Graduate Texts in Physics (Springer International Publishing, 2015).
- ²⁸Z. B. Yan and J.-M. Liu, "Coexistence of high performance resistance and capacitance memory based on multilayered metal-oxide structures," Scientific Reports **3**, 2482 (2013).