

Signal crosstalk in a flip-chip quantum processor

Sandoko Kosen,^{1,*} Hang-Xi Li,¹ Marcus Rommel,¹ Robert Rehammar,¹ Marco Caputo,²
Leif Grönberg,² Jorge Fernández-Pendás,¹ Anton Frisk Kockum,¹ Janka Biznárová,¹
Liangyu Chen,¹ Christian Krizan,¹ Andreas Nylander,¹ Amr Osman,¹ Anita Fadavi
Roudsari,¹ Daryoush Shiri,¹ Giovanna Tancredi,¹ Joonas Govenius,² and Jonas Bylander^{1,†}

¹*Chalmers University of Technology, 412 96 Gothenburg, Sweden*

²*VTT Technical Research Centre of Finland, FI-02044 VTT, Finland*

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Quantum processors require a signal-delivery architecture with high addressability (low crosstalk) to ensure high performance already at the scale of dozens of qubits. Signal crosstalk causes inadvertent driving of quantum gates, which will adversely affect quantum-gate fidelities in scaled-up devices. Here, we demonstrate packaged flip-chip superconducting quantum processors with signal-crosstalk performance competitive with those reported in other platforms. For capacitively coupled qubit-drive lines, we find on-resonant crosstalk better than -27 dB (average -37 dB). For inductively coupled magnetic-flux-drive lines, we find less than 0.13 % direct-current flux crosstalk (average 0.05 %). These observed crosstalk levels are adequately small and indicate a decreasing trend with increasing distance, which is promising for further scaling up to larger numbers of qubits. We discuss the implication of our results for the design of a low-crosstalk, on-chip signal delivery architecture, including the influence of a shielding tunnel structure, potential sources of crosstalk, and estimation of crosstalk-induced qubit-gate error in scaled-up quantum processors.

I. INTRODUCTION

The quest for demonstrating quantum computational advantage and fault-tolerant quantum computation has inspired the realisation of integrated quantum processors [1–4]. A prominent physical platform is based on superconducting qubits, which are typically sub-millimeter in size, made of lithographically defined thin-film devices on low-loss substrates, and operate at frequencies below 10 GHz in a cryogenic environment. Scaling up superconducting quantum processors requires microchip integration in an extensible design while maintaining high-fidelity qubit performance through predictable device parameters and high-yield fabrication.

An outstanding problem for extensible designs is on-chip signal routing that enables components within the processor to be selectively addressed and read out. In current technology, signals are usually routed from the edge of the chip, where wirebonds make connection to a printed circuit board and further on to connectors on a microwave package. If the signal is insufficiently shielded, crosstalk ensues and results in quantum-gate errors that render quantum computation infeasible. Active crosstalk suppression techniques, which involve characterising the crosstalk matrix and applying its inverse [5–10], are prohibitively challenging at scale. We must thus ensure that the circuit architecture supports adequate passive crosstalk suppression by proper routing and shielding techniques. Therefore, the roadmap for next-generation quantum processors requires an understanding of the influence of densely routed signal lines and an informed

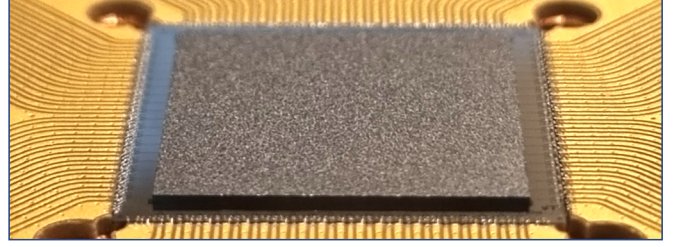


FIG. 1: A 25-qubit superconducting quantum processor packaged with wirebonds and printed-circuit board technology.

strategy for signal delivery with low crosstalk. This challenge has not received the attention it deserves.

In this work, we demonstrate packaged multi-qubit processors consisting of 25 qubits in a flip-chip module, as shown in fig. 1. The processor is designed according to a repeating signal-line routing pattern, which is, in principle, scalable to hundreds of qubits. We characterize the microwave crosstalk (selectivity of driving) of qubit drive lines (“xy-line”), which are capacitively coupled to their target qubits, and of flux lines (“z-line”), which are inductively coupled to frequency-tunable couplers that mediate two-qubit gates.

The results show crosstalk performance approaching average values of -40 dB for microwave-drive xy crosstalk and 0.05 % for direct-current flux crosstalk, competitive with reported performance from other platforms. We show that a substantial contribution to the flux crosstalk is due to the proximity of the grounded end of a target z-line to a neighbouring adversary z-line, and it can be suppressed either by a shielding tunnel structure or by adequate separation. On the other hand, enclosing the xy-lines with shielding tunnels does not improve xy

* sandoko.kosen@gmail.com

† jonas.bylander@chalmers.se

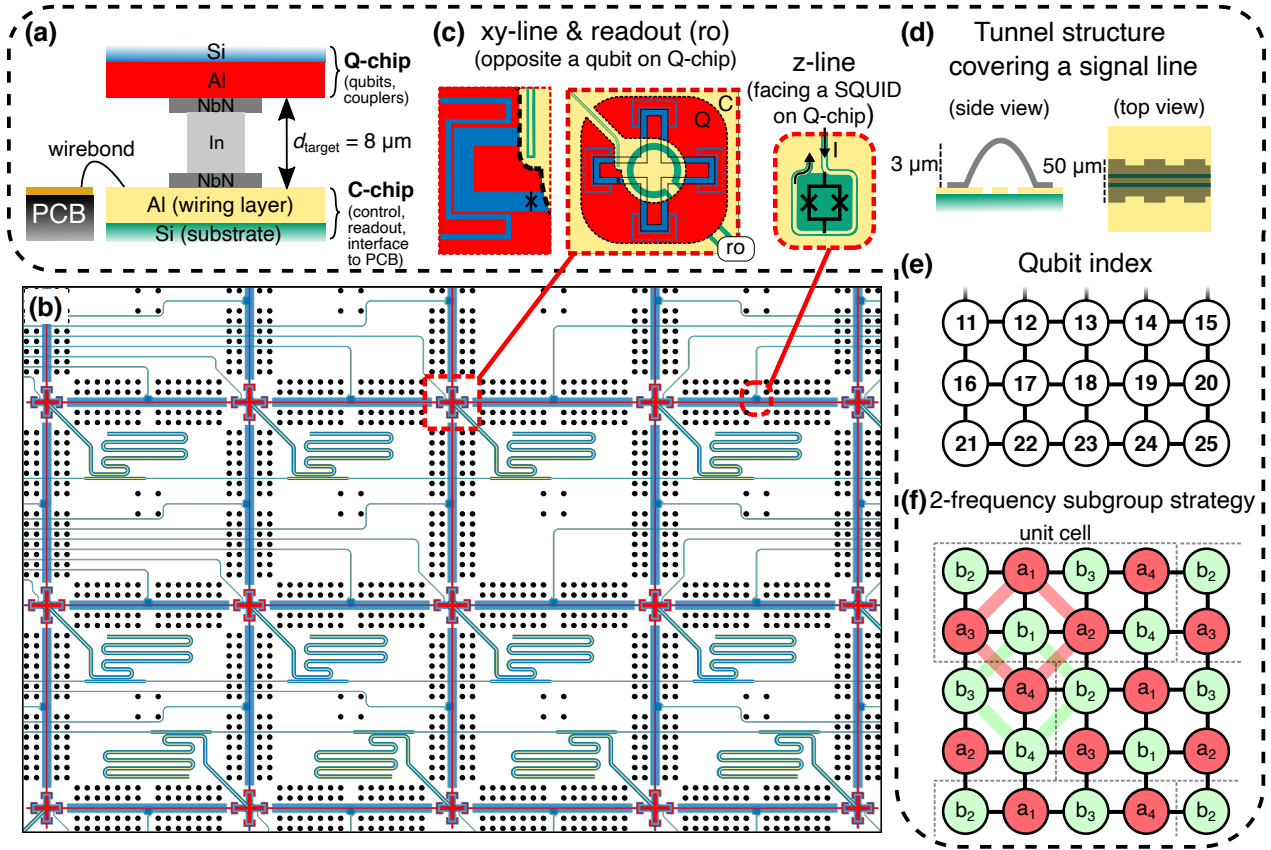


FIG. 2: Quantum processor architecture. (a) Two-tier flip-chip material stack (not to scale). (b) Overlapped view of Q-chip (qubits and couplers) and C-chip (control and readout elements) for the bottom 15 qubits of a 25-qubit QPU, showing the bump pattern (black dots). For an easier view, both ground planes are removed from this illustration. (c, left) A transmon (Xmon) qubit located on the Q-chip, with xy-line (qubit drive) and readout resonator located on the C-chip. The cutout on the Q-chip layer shows the end parts of the xy-line and of the resonator. The panel on the left shows a zoomed-in picture of the region around the tip of the xy-line. (c, right) A z-loop (flux loop) on the C-chip whose center lies directly opposite a SQUID on the Q-chip (wiring and substrate on the Q-chip not shown). (d) Aluminium tunnel structure shielding a signal line. (e) Qubit indexing used in this paper. (f) Two-frequency subgroup strategy: the two colours (red and green) indicate transmons with two different anharmonicities; a_k and b_k indicate different qubit frequencies ($a_k < b_k$), giving a total of eight different frequencies that are tiled according to the schematic.

crosstalk despite the denser routing layout, suggesting that the intrinsic crosstalk level due to direct capacitive interaction is better than the observed performance. Furthermore, there is a trend of decreasing average crosstalk level with increasing qubit separation, a feature that is favourable for the scaling-up effort. We discuss potential sources of crosstalk, provide numerical estimates for the resulting single-qubit gate error due to crosstalk in several scenarios, and discuss its implication for future design of low-crosstalk processors.

II. QUANTUM PROCESSOR ARCHITECTURE

Our superconducting quantum processing unit (QPU) consists of a two-tiered architecture [11–14] separating the circuit into a qubit chip (“Q-chip”) and a control

chip (“C-chip”), see figs. 1 and 2(a). The Q-chip comprises 25 fixed-frequency transmon (Xmon) qubits [15–17] and 40 frequency-tunable two-qubit couplers laid out on a square grid with 2 mm pitch [18]. This relatively large pitch is a choice out of convenience, since the QPU performance is limited by gate performance rather than the number of devices that can be fitted on a die. The C-chip comprises a signal delivery system routed through coplanar waveguide transmission lines on the chip surface. This signal-routing strategy is extensible to hundreds of qubits. Figure 2(b) shows a part of the flip-chip module with the Q-chip overlaid on the C-chip.

Figure 2(c) shows the control wires’ coupling points to the qubit and coupler. The qubit-readout resonators [ro in fig. 2(c)] are quarter-wavelength resonators with the open end positioned directly opposite from a qubit. The resonators are undulated to reduce coupling with neigh-

bouring couplers. The open ends of the qubit-control lines (xy) are positioned to ensure adequate capacitive coupling while minimizing Purcell decay of the qubit into its own xy-line. Finally, the coupler-control lines (z) each terminate in a loop of wire that is shorted to ground at one end without a ground plane within the loop. The current in the z-loop couples magnetic flux into the SQUID of the coupler positioned opposite the loop; this SQUID connects the coupler's island to the ground plane.

The second processor discussed in this work has aluminium tunnel structures [19] added to the C-chip, shielding the signal lines as shown in fig. 2(d). These tunnels extend across the signal lines and connect the ground planes on either side.

The Q-chip and C-chip consist of 12 mm × 12 mm and 14.3 mm × 14.3 mm silicon dies, respectively, which were aligned and joined together by flip-chip bonding with target inter-chip separation of 8 μm. The bump-bond layout is symmetrical across the dies with 2900 superconducting bumps connecting the ground planes of the two tiers, with denser distribution surrounding the qubit and coupler devices. The bumps consist of evaporated indium cylinders (25 μm wide pre-compression) with a niobium-nitride underbump metallisation layer [14].

The two-tier flip-chip module represents a straightforward method for 3D integration of QPUs, offering more flexibility for signal-wire routing and qubit-array layouts than planar layouts, with a modest increase of fabrication process complexity. It also enables the use of different fabrication processes for the two chips. In more advanced 3D-integration implementations, superconducting bumps can be used to pass signals between tiers and to provide shielding between components; hard stops (e.g. posts or pillars) can help achieve precise inter-chip separation [20, 21]; furthermore, substrates with metallised through-silicon vias (TSVs) and buried conductors can help create signal redistribution layers [22–24].

Aluminium wirebonds along the periphery of the C-chip transfer signals to and from a multilayer printed circuit board, see fig. 1. Two wirebonds are placed on every signal launchpad, and two grounding wirebonds in-between neighbouring signal lines. This wiring method works up to hundreds of wires, but begins to scale poorly beyond that, which is why ultimately higher-density interconnects and packaging solutions, e.g. ball-grid arrays or land-grid arrays, need to be adapted to superconducting QPU technology.

Our flip-chip fabrication process has been demonstrated to be compatible with qubit (transmon) coherence at the 100-μs level [14]. The wiring layer (signal and ground) on each chip is fabricated in an aluminium process, and the Josephson junctions consist of an angle-evaporated Al/AlOx/Al sandwich using the two-step Manhattan process [25, 26]. Details on the flip-chip bonding processes can be found in the supplementary material of Ref. [14].

The qubits are labelled q_i , where the index i starts in the top left corner of the chip; see fig. 2(e), which shows

q_{11} to q_{25} . The element xy_i is the corresponding xy-line for q_i . The couplers and the corresponding z-lines are labelled cp_i and z_i , where i labels the pair of coupled qubits; e.g. $cp_{(11,16)}$ is the coupler connecting q_{11} and q_{16} . The closest separation between a qubit and another xy-line (excluding its own xy-line) is about 500 μm.

The routing of signal lines is designed to be as identical as possible for these rows of qubits: q_6 to q_{10} , q_{11} to q_{15} , and q_{16} to q_{20} . The control elements (xy, z) are always routed to the desired positions from the corridor above the qubits, while the readout elements are positioned below; see fig. 2(b). The signal lines are routed horizontally to the periphery of the chip. In each corridor, there is always a z-line in-between the closest pair of xy-lines. These z-lines are needed to control horizontally oriented tunable couplers. The vertically oriented couplers, however, are controlled by z-lines that are routed side-by-side. Nearest-neighbour control lines are separated by at least 100 μm. For readout purposes, a feedthrough transmission line is routed across each corridor and is coupled to five $\lambda/4$ -resonators. Once a signal lines emerge at the qubit-array perimeter, it is routed to the closest available wirebond launchpad. For qubits in the top row (q_1 to q_5), bottom row (q_{21} to q_{25}), and the corresponding horizontally oriented couplers, the control lines are routed vertically towards the closest wirebond launchpads. No bumps or airbridge crossovers are used for signal delivery, i.e. there is no intersection of signal lines.

The allocation of qubit frequency and anharmonicity follows the two-frequency subgroup strategy designed to be compatible with implementation of parametric CZs and iSWAPs that avoids frequency collision between neighbouring couplers and minimizes crosstalk due to frequency crowding [27]. Each subgroup, labelled $\{a_k\}$ and $\{b_k\}$ ($k = 1, 2, 3, 4$), has four qubit frequencies that are distributed around a central frequency; subgroup a has lower frequencies and anharmonicities than subgroup b. The layout has a unit cell of 2×4 qubits that can be repeatedly tiled as shown in fig. 2(f). An alternative visualisation is the following: a qubit with frequency in one subgroup is pairwise coupled to qubits with frequencies in the other subgroup. Refer to Appendix C for the chosen numerical values.

The readout-resonator frequency allocation is set up to ensure that, at the targeted inter-chip separation, the qubit-resonator frequency detuning is generally between 2.1 and 2.6 GHz, which provides sufficient leeway for tolerating frequency shift in case the achieved chip separation is off-target. The coupler frequency at zero flux bias is designed to be above the readout-resonator frequency.

We designed and simulated the flip-chip QPU layout using a combination of the IBM Qiskit Metal design toolkit [28], ANSYS electromagnetic simulation software [29], and L-Edit layout editor [30]. The simulation technique for individual qubits and resonators is described in Ref. [14].

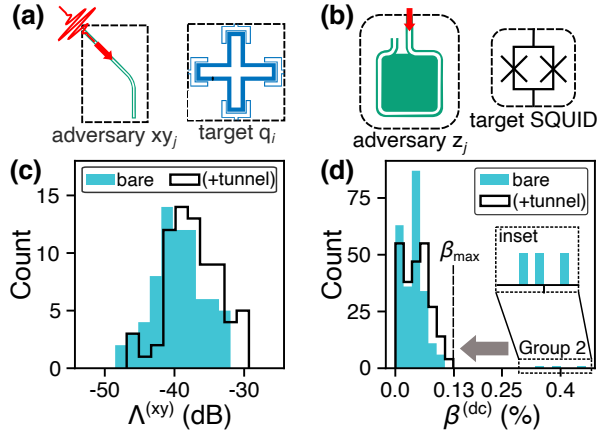


FIG. 3: Aggregate performance of xy crosstalk $\Lambda^{(xy)}$, and dc-flux crosstalk $\beta^{(dc)}$. (a) Illustration of xy crosstalk from an adversary xy-line (j) to another target qubit (i), and (b) dc-flux crosstalk from an adversary z-line (j) to another target coupler's SQUID loop (i). (c) Histogram of the on-resonant xy crosstalk, $\Lambda_{i,j}$, measured on 72 pairs for one flip-chip module with bare transmission lines (labelled “bare”), and another module with a majority of the transmission lines covered by “tunnel” structures (labelled “+tunnel”). (d) Histogram of the dc-flux crosstalk, $\beta^{(dc)}$, measured on 240 pairs. Data indicated as Group 2 are associated with a subset of pairs whose z-lines are nearest neighbour. With the tunnels, the maximum value of dc-flux crosstalk drops to $\beta_{\max} = 0.13\%$.

III. AGGREGATE CROSSTALK PERFORMANCE

Here we quantify the crosstalk (unintended driving) affecting qubits and couplers due to signals applied to the circuit's various xy-lines and z-lines, respectively. To begin with the microwave crosstalk of xy-lines, consider any pair of a target qubit (victim, q_i) and an adversary xy-line ($xy_{j \neq i}$) as shown in fig. 3(a). The crosstalk is quantified by the rotation of the quantum state vector of q_i due to a signal being delivered through xy_j aiming to control its corresponding qubit q_j . In practice, we compare the Rabi frequency of the target qubit, $\Omega_{i,j}$, with that of the qubit of the adversary xy-line, $\Omega_{j,j}$, for the same xy_j signal amplitude. Due to the low-crosstalk nature, we always drive the target qubit on resonance. Their ratio, expressed in decibel (dB), is the on-resonant xy crosstalk $\Lambda_{i,j}$ (referred to as xy selectivity in [31]),

$$\Lambda_{i,j} = 10 \times \log_{10} \left(\frac{\Omega_{i,j}}{\Omega_{j,j}} \right)^2. \quad (1)$$

The lower the magnitude of $\Lambda_{i,j}$, the better that xy-line is at selectively driving its corresponding qubit compared to any other qubit (lower crosstalk).

We also characterise the magnetic-flux crosstalk in the z-lines by examining changes in the magnetic flux ($\Delta\Phi_i$) that threads the SQUID of a target coupler cp_i due to

direct-current (dc) or alternating-current (ac) signals on an adversary z-line ($z_{j \neq i}$), aimed to control its corresponding coupler cp_j , see fig. 3(b). The magnetic-flux crosstalk is defined as [32]

$$\beta_{i,j} = \left| \frac{\Delta\Phi_i}{\Delta\Phi_j} \right|. \quad (2)$$

Generally, $\Phi_i = \Phi_i^{(dc)} + \Phi_i^{(ac)} \cos(\omega_i^{(ac)}t + \theta_i)$, where $\omega_i^{(ac)}$ is the angular frequency of the ac-flux drive signal and θ_i is its phase offset. In practice, the dc-flux and the ac-flux crosstalks, i.e. $\beta_{i,j}^{(dc)}$ and $\beta_{i,j}^{(ac)}$, are characterised separately.

The measurement procedures for the xy, dc-flux, and ac-flux crosstalks are discussed in Appendix B. As there are also some defective elements in these first-generation processors, the datasets presented in this section are only associated with target-adversary pairs that are functional in both processors (bare waveguides and with tunnels) to allow fair comparisons. The complete datasets can be found in Appendix E.

Our results show that the decrease in xy crosstalk due to the addition of tunnel structures is not statistically significant. Figure 3(c) shows a histogram of the xy crosstalk $\Lambda^{(xy)}$ measured both without and with tunnels, with average values -39.4 ± 3.7 dB and -37.4 ± 3.9 dB, respectively.

Figure 3(d) shows a histogram of the dc-flux crosstalk $\beta^{(dc)}$ measured both without and with the tunnel structures. Statistics from both data sets show average values of approximately 0.05%. Data from the processor without the tunnels has outliers in-between 0.3% and 0.6% (indicated as Group 2), which originate from pairs whose z-lines are not only nearest neighbour but also arranged in a specific way (see section IV). These outliers are not present in the data from the processor with the tunnel structures, indicating a suppression of dc-flux crosstalk; here, the maximum measured value is 0.13%.

As the ac-flux crosstalk $\beta^{(ac)}$ measurement is more involved, we only characterised it for Group-2 pairs of z-lines and couplers, i.e. those that exhibited elevated dc-flux crosstalk in the absence of tunnels. We chose to characterise it at a signal frequency of 200 MHz, close to the typical modulation frequency of our parametric couplers. Similarly to dc-crosstalk, the largest ac-crosstalk drops from 0.85% to 0.24% for tunnel-covered z-lines.

In the next section, we examine the distance dependence of the $\Lambda^{(xy)}$, $\beta^{(dc)}$, and $\beta^{(ac)}$ data.

IV. CROSSTALK VS. DISTANCE

During the operation of a quantum processor, gate operations on different qubits and couplers will be performed simultaneously via multiple signal lines. It is therefore important to design the QPU such that the crosstalk decreases for larger separation. Such a property allows reusing the qubit parameters from one unit

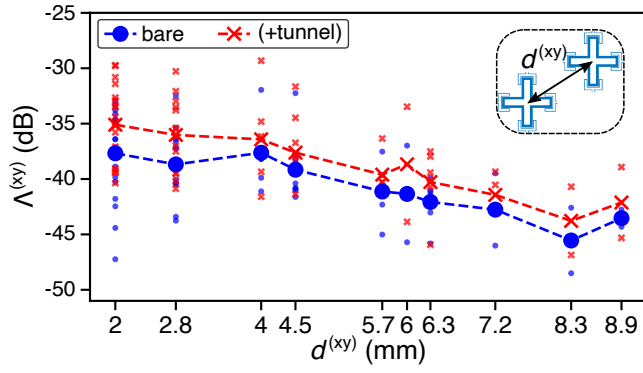


FIG. 4: Distance dependence of the xy crosstalk, $\Lambda^{(xy)}$. The distance $d^{(xy)}$ is defined as the separation between the qubit of the adversary xy-line and the target qubit. The scatter plot indicates the distribution of $\Lambda^{(xy)}$ data for each $d^{(xy)}$, and the larger symbols denote the average.

cell in another as part of our qubit-frequency allocation scheme; see fig. 2(f). It also ensures that the total error due to signal crosstalks remains sufficiently small. In this section, we begin to address this by demonstrating smaller average crosstalk for larger separations.

We sorted the $\Lambda^{(xy)}$ data in fig. 3(c) according to the distance $d^{(xy)}$ between the target qubit and the qubit of the adversary xy-line (or the adversary qubit); the results are shown in fig. 4. It should be pointed out that there are fewer data points for larger $d^{(xy)}$ in fig. 4, i.e this is natural for the planar connectivity such as the one implemented in our processors. The dashed lines connecting average $\Lambda^{(xy)}$ values ($\bar{\Lambda}^{(xy)}$), indicated by larger symbols of circles and crosses) hint at a trend of decreasing $\bar{\Lambda}^{(xy)}$ with $d^{(xy)}$. Fitting the average values with an empirical linear model (see Appendix F) yields a slope of approximately -1 dB/mm for these processors.

For the flux crosstalk, we focus specifically on two layouts of neighbouring z-lines as shown in fig. 5(a,b). The first layout consists of the set $\{A, B, C\} = \{z_{(11,16)}, z_{(12,17)}, z_{(13,18)}\}$, and the second consists of $\{A', B', C'\} = \{z_{(16,21)}, z_{(17,22)}, z_{(18,23)}\}$. The two layouts are very similar: most of the lines are nearest neighbours, beginning from the wirebond launchpads and leading all the way to the target position (see chip layout in fig. 2). The only major difference is in the third z-line: C' is routed on the *upper* side of A' and B' , while C is routed on the *lower* side of A and B . The data with C' as target from the processor with tunnels is not available due to a defective SQUID in coupler $cp_{(18,23)}$.

On the first layout without the tunnel structure, fig. 5(a), the highest crosstalk β (dc: 0.44%, ac: 0.58%) appears with A as the target and B as the adversary line. However, a much lower crosstalk (dc: 0.06%, ac: 0.10%) appears between target B and adversary C despite being nearest-neighbour lines in the same way as target A and adversary B . Almost similar results are observed on the second layout in fig. 5(b), with the exception that sub-

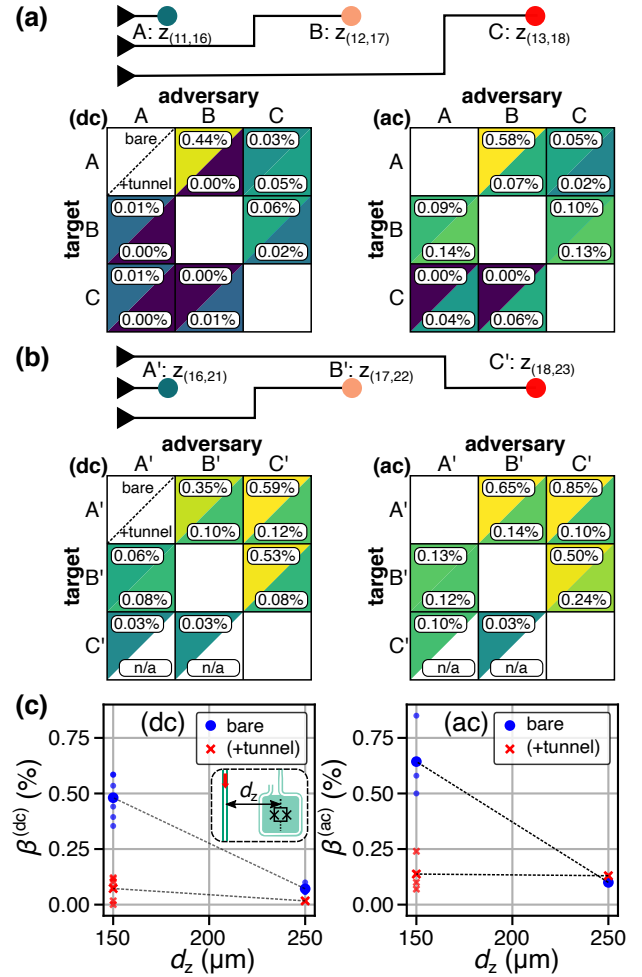


FIG. 5: Layout-dependent flux-crosstalk behaviour. (a,b) Detailed comparisons of flux crosstalk for two different configurations of nearest-neighbour z-lines. The darker the background colour, the smaller the crosstalk. (c) Distance dependence of flux dc and ac crosstalk for pairs of adversary-target arranged as shown in the inset, where the red arrow indicates the adversary current. The dashed lines connecting the data points are meant to guide the reader's eyes.

stantial crosstalk is also observed between target A' and adversary C' (also between target B' and adversary C').

Another noteworthy feature is the asymmetry of crosstalk for nearest-neighbour lines. The effect is most pronounced for the processor without tunnels. Whereas there is a substantial crosstalk from adversary B to target A (dc: 0.44%, ac: 0.58%), a much lower crosstalk is measured when the roles of target and adversary are interchanged (dc: 0.01%, ac: 0.09%). Similar asymmetry is observed in the other layout.

These observations, combined with the symmetric positioning of the wirebond launchpads of the z-lines, indicate that the major source of flux crosstalk in the processor without tunnels is coming from the proximity of the end (current loop) of a target z-line and the nearest section of an adversary z-line. Under this model, we plotted

flux crosstalk for pairs of target–adversary arranged as shown in the inset of fig. 5(c). Without tunnels, the flux crosstalk becomes smaller for larger spatial separation d_z . By adding tunnels, the previously high flux crosstalk at small separation ($d_z = 150\ \mu\text{m}$) decreases by close to 10 times, down to the level of 0.1–0.2 %. Flux crosstalk at larger separation ($d_z = 250\ \mu\text{m}$) is relatively unaffected by the presence of tunnels.

V. DISCUSSION

A. Qubit-drive crosstalk

A distinct feature in this processor is the presence of densely routed signal lines in the proximity of qubits within the flip-chip environment; see fig. 2(b). However, for xy crosstalk, direct capacitive interaction between qubits and these signal lines cannot be the dominant mechanism, since we do not observe any decrease in crosstalk after covering the xy-lines with shielding tunnel structures; see figs. 3(c) and 4.

The average of $\Lambda^{(\text{xy})}$ is $-36\ \text{dB}$ for the nearest-neighbour pairs ($d^{(\text{xy})} = 2.0\ \text{mm}$) and $-37\ \text{dB}$ for the next-nearest-neighbour pairs ($d^{(\text{xy})} = 2.8\ \text{mm}$). The highest values are $-30\ \text{dB}$ for both nearest and next-nearest neighbours. This performance compares favourably with results from a 17-qubit processor (in a single-chip geometry) employed in Ref. [33] for the demonstration of distance-three quantum error correction. There, the highest crosstalk among the reported values for next-nearest-neighbour qubit ($d^{(\text{xy})} = 2.4\ \text{mm}$) was $-20\ \text{dB}$ (excluding one outlier at $-4\ \text{dB}$). It is not straightforward to identify the factors that led to the lower xy-crosstalk level demonstrated in our work despite having a denser signal-line layout. However, there are good reasons to believe that the chip geometry is important. The electric field of a coplanar waveguide is more confined in a flip-chip geometry than in a planar chip, due to the presence of a ground plane on the opposing chip (the typical size of a transmission line is $\sim 10\ \mu\text{m}$, and our chip separation is $8\ \mu\text{m}$) [14]. In a single planar chip, additionally, the signal lines can interact parasitically with qubits via the field in the substrate, whereas in our flip-chip module, signal lines and qubits are separated onto different chips.

The data for $\Lambda^{(\text{xy})}$ are sorted according to qubit-qubit distance $d^{(\text{xy})}$ in fig. 4 purely for a scaling argument. We believe that for a signal delivery architecture to be scalable, not only should $\Lambda^{(\text{xy})}$ decrease with $d^{(\text{xy})}$, but the behaviour should not be too dependent on the architecture itself. Such a behaviour would not only unlock favourable scaling behaviour, it would also simplify the hardware design process by reducing the number of factors that need to be accounted for. When combined with a judicious choice of qubit-frequency allocation and a substantial decrease in $\Lambda^{(\text{xy})}$ for increasing $d^{(\text{xy})}$, it can lead to very low total crosstalk error. Having said that,

the relatively large spread of $\Lambda^{(\text{xy})}$ for every qubit-qubit distance $d^{(\text{xy})}$ in fig. 4 provides a clue that the major parasitic interaction in our processors does not have a strong dependence on $d^{(\text{xy})}$. The dominant source of crosstalk must therefore be sought elsewhere. Nevertheless, there is a hint of lower crosstalk for larger separation when comparing the average value of $\Lambda^{(\text{xy})}$ versus $d^{(\text{xy})}$, suggesting a favourable scaling behaviour, at least for the size of processors examined in this work.

An alternative to flip-chip geometry called the “coax-mon” reported nearest-neighbour ($d^{(\text{xy})} = 2\ \text{mm}$) crosstalk $\Lambda^{(\text{xy})} \sim -56\ \text{dB}$, roughly 20 dB better than the result reported in this work [31]. This was obtained using a smaller 2×2 qubit chip ($5 \times 5\ \text{mm}^2$) in an enclosure that is inductively shunted at the center to repel the cavity modes to higher frequencies, an additional feature that is yet to be present in our system. It will be interesting to compare crosstalk performance between the two geometries for increasing processor size.

Electromagnetic modelling of the whole system (chips, wirebonds, packaging) is computationally challenging due to the wide range of feature sizes (several micrometers for signal lines to several centimeters for the packaging) and is therefore not pursued in this work. However, numerical validation is important going forward to quantitatively understand xy crosstalk.

The xy-crosstalk performance of our quantum processors compares competitively with those demonstrated in trapped ions [34–40], neutral atoms [41–43], and spin qubits [44, 45]. In trapped-ion systems, the lowest nearest-neighbour crosstalk (without active cancellation) was reported to be 0.2 % for a linear chain of four $^{171}\text{Yb}^+$ ions, which is equivalent to an individual excitation-error probability of 10^{-5} [37]. In our case, the qubit-frequency allocation strategy results in nearest-neighbour qubits that are naturally far detuned. For $\Omega_R/2\pi = 25\ \text{MHz}$, and with the smallest nearest-neighbour detuning being 420 MHz, the individual excitation-error probability is already at the level of 10^{-6} ; larger detuning will further reduce the signal-crosstalk-induced error probability. Neutral-atoms systems have reported an average spin-flip crosstalk probability of 2×10^{-3} on a two-dimensional array of 49 Cs atoms [41]. Spin-qubit systems, such as the four-atom Ge processor in Ref. [45], show an average individual single-qubit gate error between 10^{-2} and 10^{-4} .

B. Flux crosstalk

The flux-crosstalk data [fig. 5(a,b)] clearly illustrate specific configurations of z-lines that cause some of the largest flux-crosstalk values measured in our processors (between 0.4 and 1 %). We demonstrated two strategies to achieve lower flux crosstalk. The first strategy uses a tunnel structure to suppress crosstalk for the same pairs of z-lines below $\sim 0.2\ \%$. This conclusion is only made possible due to the use of identical signal-line footprints in the two devices. The second strategy is by ensuring a

sufficiently large separation d_z between the head of the target z-line and the closest point of an adversary z-line, in our case $d_z = 250 \mu\text{m}$. Further investigation is needed to pinpoint precisely the cause of crosstalk reduction due to the tunnel structure: whether the tunnel prevents current leakage to the target z-line and/or if it suppresses the direct interaction between the adversary z-line and the target SQUID.

The average dc-flux crosstalk $\beta^{(\text{dc})}$ over all measurable pairs is $\sim 0.05\%$. At least another tenfold reduction is possible through active flux compensation, potentially pushing the dc-flux crosstalk level below 0.01% . A similar reduction has also been demonstrated in a 16-qubit processor [8]. Note that the passive stability of our system is much better: a variation of $32 \mu\Phi_0$ is measured for one of the z-lines over a period of 3 hours, corresponding to a lowest measurable $\beta^{(\text{dc})} = 0.003\%$. See Appendix B 2 for more information.

There is a varying degree of tolerable $\beta^{(\text{dc})}$ performance. An active flux-calibration technique applied to devices for quantum-annealing applications achieves maximum calibration error of 0.17% [5], which is still higher than the passive performance already obtained by our architecture. In another work employing a superconducting quantum simulator to study many-body dynamics, $\beta^{(\text{dc})}$ was reduced from 6% down to 0.01% through active compensation [9].

Overall, this work demonstrates that careful routing and shielding of z-lines can already enable low crosstalk without active flux compensation. The crosstalk performance can be compared with various leading devices (flip-chip, single-chip) where the maximum flux crosstalk (no compensation) varies between 0.8% and 40% [5, 9, 32, 33, 46–48]. Authors in Refs. [47, 48] noted an improvement in maximum flux crosstalk down to the level of 1.6% when moving from single-chip to flip-chip geometry on nominally similar chip sizes, attributed to the use of a smaller SQUID area. Meanwhile, Ref. [33] already registered a maximum flux crosstalk of 0.8% on a single-chip geometry, lower than those achieved in Ref. [48]. The use of airbridge crossovers meant to stitch the ground plane of a z-line did not immediately result in full crosstalk reduction as demonstrated by Ref. [46], where the authors measured flux crosstalk between 0.1% and 4% . Finally, we note that Ref. [49] obtained $\beta^{(\text{dc})} = 0.8\%$, despite using a z-line with a dedicated return-current line. This illustrates the complex story of flux-crosstalk improvement efforts, and the signal-line architecture presented in this work is a proof that lower crosstalk is still possible to achieve via careful design. Further investigations are required to understand the source of flux crosstalk at the 0.1% level.

C. Impact on gate fidelities

It is instructive to understand the detrimental effect of the xy-crosstalk performance on the single-qubit gate

fidelity. In previous work, we calculated the fidelity using the relative coupling strength between the relevant processes and detuning between the associated transitions [27]. The calculation models the qubits as two-level systems and assumes that the crosstalk activates undesired processes one by one. The measured $\Lambda^{(\text{xy})}$ varies between -56 dB and -27 dB , which corresponds to relative coupling strengths between 0.15% and 4% . Assuming a 20 ns single-qubit gate, the worst $\Lambda^{(\text{xy})}$ of -27 dB would require detuning between the relevant qubit transitions larger than 28 and 42 MHz (about 1% of typical qubit frequencies) to have average gate fidelities above 99.9% and 99.99% respectively.

The limits are more stringent when we consider influence from all other qubits on the chip. We examine the total single-qubit gate fidelity F_{1Q} for increasing processor size. We assume an empirical linear behaviour of $\bar{\Lambda}^{(\text{xy})}$ on $d^{(\text{xy})}$ and numerically simulate the impact on F_{1Q} under certain assumptions (see Appendices F, G, H). For the data in fig. 4, the slope m_{xy} and intercept Λ_0 values of the empirical linear model are approximately -1 dB/mm and -34 dB , respectively. The simulations suggest, for QPUs with up to 1000 qubits, that an improvement to -2.0 dB/mm and -50 dB would result in a total single-qubit gate error (due to xy crosstalk) well below the 0.1% threshold recommended for quantum error correction using the surface-code [50]. This conclusion assumes linear dependence of $\bar{\Lambda}^{(\text{xy})}$ vs $d^{(\text{xy})}$ for processor sizes beyond the one measured in this work. We have no reasonable physical argument to assume that it will be the case; nevertheless, this number can serve as a guide for future hardware development and can hopefully spur further effort in verifying this relation for larger processors. Note that a sparser lattice architecture, such as the heavy square or the heavy hexagon, will benefit from less stringent criteria due to fewer neighbouring qubits and more relaxed frequency constraints [51].

It is more challenging to analyze the influence of flux crosstalk on the two-qubit gate fidelity since the gate strength depends on both the dc bias and the ac amplitude in a nontrivial way ($\omega_{\text{cp}}(\Phi)$ is non-linear). However, there is a relevant situation for which the analysis becomes simpler, at least qualitatively: a parametric gate is applied to a coupler while the other ones idle. Two related conditions arise in that case: (1) the driving amplitude produced on the idling couplers will be very small for low crosstalk such as the one measured in this work, allowing for a perturbative expansion, and (2) the dc contribution stemming from the periodic modulation will be negligible, as it is a higher-order effect in the small-amplitude perturbative expansion. Furthermore, as the dc bias usually stays untouched during the parametric-gate operation, the effect of dc crosstalk on the idling couplers should not change during the gate operations.

An expression for the first-order contribution to the gate strength of the iSWAP gate is known for this small-amplitude expansion [52], although the result is limited to the regime where the detunings between the cou-

pler and the qubits are much larger than their coupling strengths. The expression clearly shows that the gate strength is less sensitive to changes in both ac amplitude and dc bias near the zero-flux bias region. This region is also where the couplers are typically more far-detuned from the qubits, thus avoiding the physical consequences of being near avoided level crossings, i.e. Rabi oscillations or extra phase acquisition. Therefore, the general prescription to avoid big impact of crosstalk during the application of parametric gates would be to idle the other couplers to be as far detuned as possible from the neighboring qubits.

VI. CONCLUSION AND OUTLOOK

We demonstrated superconducting quantum processors utilising an on-chip signal-delivery architecture with competitive crosstalk performance — average on-resonant xy crosstalk ~ 40 dB, average dc-flux crosstalk $\sim 0.05\%$ — surpassing a majority of those demonstrated in other physical platforms. The systematic comparison enabled by adding a tunnel structure on an identical signal-line footprint shows that the direct capacitive interaction between densely routed signal lines and the qubits are not the main contributor to the xy-crosstalk level in these processors. Our work demonstrates wiring layouts that can lead to flux crosstalk at the $\sim 1\%$ level and strategies to reduce it down to $\sim 0.1\%$.

Further investigations into the source of crosstalk would be required before proposing reliable mitigation strategies; the lists below are non-exhaustive. For xy crosstalk, there are at least three possible avenues to investigate. The first is the direct crosstalk between signal lines (including the wirebonds) both within the substrates and outside the flip-chip region as well as on the printed circuit board. The second is to electromagnetically simulate the direct capacitive interaction between a target qubit and the entire length of an adversary signal line (including the wirebonds). The third is to investigate the role of packaging cavity modes in influencing these two crosstalk mechanisms, as suggested in Ref. [53]. For flux crosstalk, it will be instructive to investigate if it is limited by the leakage of the return current into the target line (around the launchpads or the area around the SQUID), or if the return current is contributing non-negligible magnetic flux at the location of the target SQUID.

More advanced signal-delivery architectures will benefit from the use of on-chip signal multiplexers, bumps, and especially redistribution layers enabled by through-silicon vias (TSV) in a multi-tiered stack [22–24, 54, 55]. Bumps and TSVs are typically a few tens of micrometer in size, which is relatively large compared to typical transmission lines. It remains to be seen the extent to which they influence the overall signal-crosstalk level.

The low crosstalk demonstrated in this work and other cited works highlights the strength and flexibility af-

forded by superconducting circuit architectures. There is still no clear lower limit for the achievable passive crosstalk performance via further system design. We hope to inspire further efforts and discussion in the quantum hardware community, both within and outside superconducting platforms, to investigate the source of crosstalk as well as its behaviour as systems scale up in size.

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AUTHOR CONTRIBUTION

SK planned and performed the experiments, analysed the data, and produced the numerical simulations. SK and HXL designed the QPU with inputs from MR, RR, JFP, AO, AFR, DS, AFK, GT, and J.Byl. MR, SK, AN, and HXL fabricated the control and quantum chips with inputs from J.Biz, AO, and AFR. MC and LG formed the In bumps and performed the flip-chip bonding. RR, GT, and SK developed the QPU packaging. CK assisted with the writing of measurement instrument drivers. SK, LC, CK, HXL, and GT set up and maintained the measurement and cryogenic facilities. SK and J.Byl wrote the manuscript with input from all authors. GT, JG, and J.Byl supervised the project.

COMPETING INTERESTS

RR, GT, and SK are co-founders and shareholders of Scaling AB. Other authors declare no competing interests.

DATA AVAILABILITY

The data that support this work are available from the corresponding author upon reasonable request.

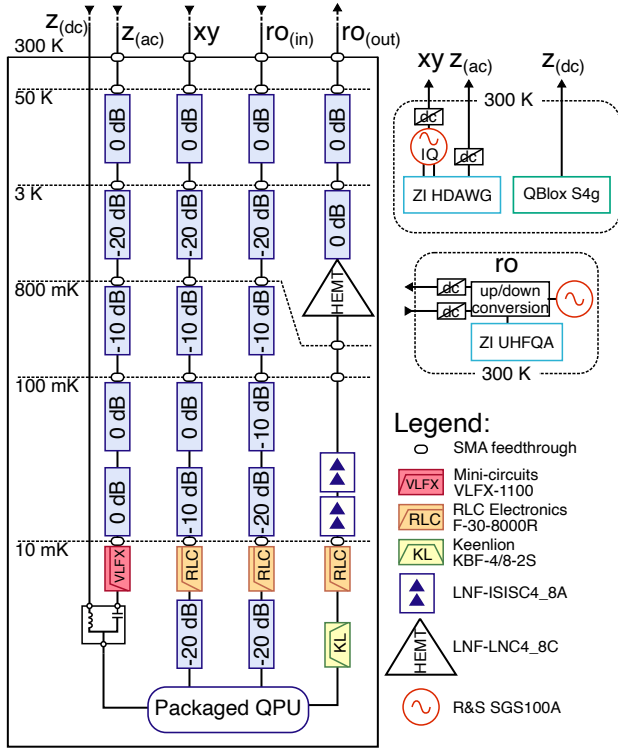


FIG. 6: Measurement apparatus at cryogenic and room temperature.

Appendix A: Experimental setup

Figure 6 shows the measurement apparatus employed in this work at cryogenic and room temperature.

Appendix B: Measurement techniques

1. xy crosstalk

The xy crosstalk $\Lambda_{i,j}$ [eq. (1) in the main text] is the ratio of the on-resonant Rabi frequencies squared, i.e. $(\Omega_{i,j}/\Omega_{j,j})^2$, expressed in decibel for a fixed drive amplitude V_j ; see fig. 3(a). We obtained a series of Rabi frequencies for various drive amplitudes [fig. 7(a)] and fitted the data with a linear relation $\Omega_{i,j} = k_{i,j}V_j$ to obtain the slope $k_{i,j}$. We obtained $k_{j,j}$ in a separate measurement. $\Lambda_{i,j}$ is then equal to the ratio $(k_{i,j}/k_{j,j})^2$ expressed in decibel.

We operated the radio-frequency (rf) source (Rohde & Schwarz SGS100A) in IQ modulation mode. We fixed its output power to 14 dBm and varied the amplitudes V_j of the signals sent to its IQ input ports. For each V_j , we obtained a Rabi oscillation and fitted it with an exponentially decaying sinusoidal function. Figure 7(a) shows $\Omega_{i,j}$ and $\Omega_{j,j}$ vs. V_j for $i = 15$, $j = 14$.

In the measurement of $\Lambda_{i,j}$, we took into account the frequency dependence of the transmission of the cables and components, measured using a vector network anal-

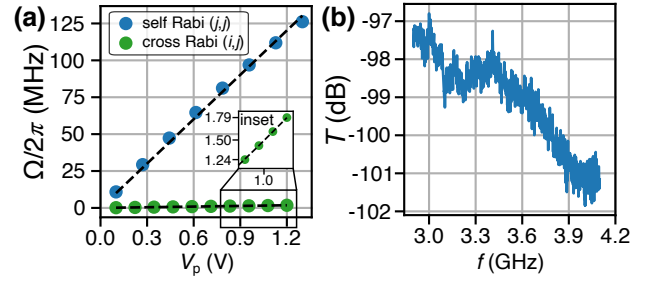


FIG. 7: xy-crosstalk measurement. (a) Measured Rabi frequencies as a function of the drive amplitude for the self-drive ($i = j$) and cross-drive ($i \neq j$). (b) An example of combined output and transmission characteristics of an rf source with the cables and components all the way down to the PCB level (measured at room temperature).

yser at room temperature. We measured the output characteristic of the rf source for different frequencies with a spectrum analyser (Rohde & Schwarz FSL18, frequency span 1 MHz, intermediate frequency bandwidth 10 KHz, 20 averages, 101 points). Figure 7(b) shows an example of the transmission characteristic of the cables and components.

2. dc-flux crosstalk

The first step in the characterisation of flux crosstalk is to relate the z-line's direct current (dc) I with the magnetic flux $\Phi^{(dc)}$ applied to the SQUID of the coupler; see figs. 2(c) and 3(b). This is done via continuous-wave (cw) frequency spectroscopy of the neighbouring qubit (which is coupled to the target coupler) as shown in fig. 8(a). When the coupler comes close to resonance with the qubit, we observe an avoided crossing. By identifying a series of such crossings, we are able to deduce the current required to apply one flux quantum to the SQUID, as well as the dc offset current corresponding to the true zero dc-flux bias on the SQUID. In our case, one flux quantum ($\Phi_0 = 2.067 \times 10^{-15}$ Wb) corresponds to approximately 3 mA.

To measure dc-flux crosstalk $\beta_{i,j}^{(dc)}$ [eq. (2) in the main text], the target coupler cp_i is first biased close to one such avoided crossing. In the absence of a dedicated coupler-state readout resonator, this is a sensitive region to probe $\beta^{(dc)}$ through qubit-state readout. A small shift in the frequency of cp_i , from f_p to f'_p , can be inferred from the change in the hybridised coupler-qubit frequency f_p , imparted by the adversary current I_j . In an ideal condition with zero crosstalk, i.e. $\beta_{i,j}^{(dc)} = 0$, f_p is independent of the value of the current I_j applied on adversary z_j . Due to non-negligible crosstalk, f'_p will slightly shift as a function of I_j , and the goal is to find the new current value I'_i that restores f'_p to f_p . In practice, we fixed the qubit probe frequency f_p (typically ~ 10 MHz away from the qubit bare frequency), and determined I'_i

for three different dc currents I_j corresponding to adversary coupler (cp_j) flux bias values $-\Phi_0$, 0, and Φ_0 ; see fig. 8(b). We obtained $\beta_{i,j}^{(dc)}$ by converting I_i' to the corresponding flux applied on z_i .

Figure 8(c) demonstrates the passive stability of the dc-flux environment of a z-line for 3 hours. We repeatedly swept the input current to the z-line while maintaining the same probe frequency. From the positions of the extracted peak, we obtained a standard deviation of the variation of the current to be $32 \mu\Phi_0$, or equivalently 100 nA, which is smaller than the minimum step in output current allowed by the source (~ 380 nA). Furthermore this is much smaller than the typical dc-flux crosstalk observed in our system, which is around $500 \mu\Phi_0$ when $1\Phi_0$ is applied to the adversary z-line.

Figure 8(d) demonstrates active dc-flux compensation on one of the target z-lines using the obtained crosstalk coefficient. As the dc-flux on the adversary line is varied between $-\Phi_0$ and Φ_0 , the range in which the signal peak drops more than tenfold: from 7.12 MHz to 0.53 MHz. Further studies are required to understand this number and optimise the crosstalk-calibration procedure to push it below the limit allowed by the measurement setup.

3. ac-flux crosstalk

For the case of ac-flux crosstalk, interference between ac-flux signals applied to the target z-line and parasitic signals from the adversary z-line renders the technique used for dc-flux crosstalk measurement inapplicable. Instead, we employ a modified Ramsey pulse sequence following Ref. [32]. We first give an overview of this technique before describing the calibration and measurement steps leading up to the crosstalk data.

First, consider a qubit-coupler system (q_i, cp_i). The original Ramsey pulse sequence consists of two frequency-detuned $\pi/2$ -pulses on the qubit, separated by an idle time Δt ; see fig. 9(a). By measuring the q_i population as a function of Δt , we obtain a Ramsey fringe whose oscillation frequency $\delta\omega = \omega_i^q - \omega_{\text{drive}}$ corresponds precisely to the detuning between the applied pulse and the actual frequency of q_i . In the modified Ramsey pulse sequence, an ac-flux pulse at angular frequency $\omega_i^{(ac)}$ is also applied to the coupler, via z_i , during that idle duration, as shown in fig. 9(a). This ac-pulse modulates the qubit frequency and consequently also the detuning, which makes the observed $\delta\omega$ sensitive to the applied ac-flux pulse amplitude.

Now we modulate the target coupler cp_i through an adversary line z_j to quantify the ac-flux crosstalk $\beta_{i,j}^{(ac)}$. The target coupler is biased at specific dc-flux and ac-flux bias points (angular frequency $\omega_i^{(ac)}$, phase θ_i) chosen to render it susceptible to detecting parasitic ac-flux signals. An ac-flux signal on an adversary line z_j , at frequency $\omega_j^{(ac)} = \omega_i^{(ac)}$, will cause a noticeable shift in $\delta\omega$ obtained via the modified Ramsey pulse sequence. We measure

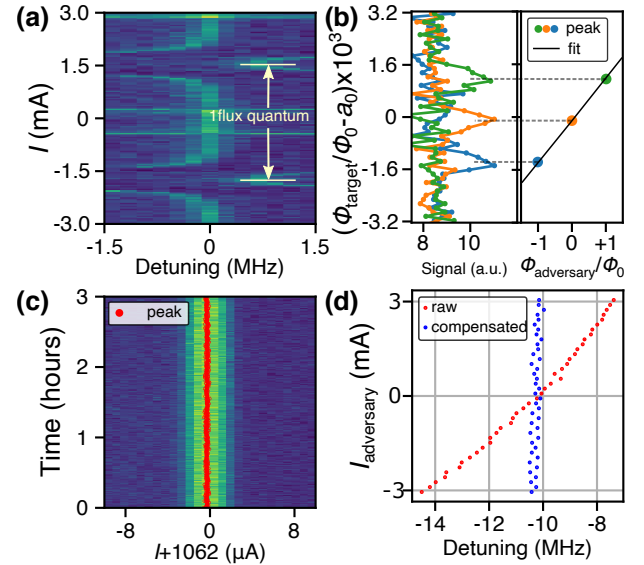


FIG. 8: dc-flux crosstalk measurement. (a) Qubit-frequency spectroscopy vs. current I applied to a neighbouring tunable coupler. Detuning refers to the frequency difference between the probe tone and the qubit at $I = 0$. The avoided-crossing regions are used to probe for small shifts in the coupler frequency due to qubit-coupler hybridization. The “1 flux quantum” label refers to the magnetic-flux periodicity of the coupler frequency. (b) Shift in the flux Φ_{target} of the target coupler vs. flux $\Phi_{\text{adversary}}$ of the adversary coupler. Each curve in the left panel represents a narrow vertical slice of the data in (a) around the vicinity of one of the avoided crossings ($a_0 = 0.365696$). For each $\Phi_{\text{adversary}}$, we extracted Φ_{target} as shown in the right panel. The slope yields the dc-flux crosstalk coefficient (here $|\beta_{i,j}| = 0.13\%$). (c) Repeated qubit-frequency spectroscopy for 3 hours to demonstrate the stability of the system. Here, we fixed the probe frequency and varied the current I at the neighbouring coupler. (d) Demonstration of active dc-flux compensation by subtraction of the crosstalk.

$\delta\omega$ for a range of phase offsets $\Delta\theta = |\theta_j - \theta_i|$ spanning $[0, 3\pi]$, as shown in fig. 9(e). The maximum swing of $\delta\omega$ (or $\Delta(\delta\omega)$) corresponds to an equivalent ac-flux shift in cp_i : $\Delta\Phi_i^{(ac)} = 2\beta_{i,j}^{(ac)}\Phi_j^{(ac)}$.

In practice, we proceeded with the following steps: (1) relate $\Phi^{(ac)}$ to the ac-voltage amplitude $V^{(ac)}$ applied by the instrument, (2) make a choice of dc- and ac-flux bias points for the target cp_i , (3) apply a large ac-flux signal on the adversary z_j , (4) run the sequence in fig. 9(a) and relate the measured swing $\Delta(\delta\omega)$ to $\Delta\Phi_i^{(ac)}$ at the bias point, which in turn enables the determination of $\beta_{i,j}^{(ac)}$.

To relate $V_i^{(ac)}$ to $\Phi_i^{(ac)}$ for any pairs of z_i and cp_i , we ran the ac-flux calibration pulse sequence in fig. 9(a). Figure 9(b) shows the measured Ramsey fringes for a range of voltages $V_i^{(ac)}$. Next, we ran a Qutip simulation [56, 57] of this pulse sequence using the measured parameters of qubit, qubit drive, and the coupler zero-

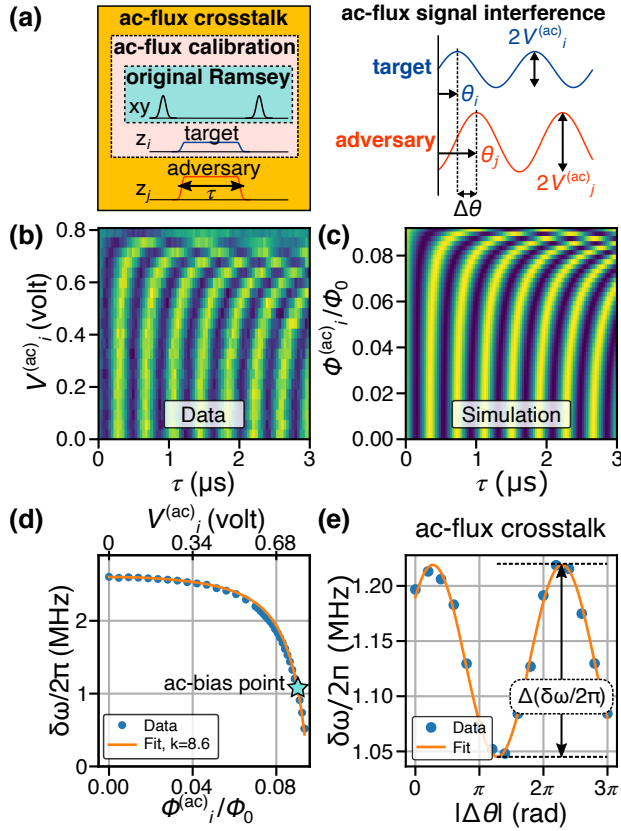


FIG. 9: ac-flux crosstalk measurement. (a) Control pulse sequence. (b) Data obtained from running the ac-flux calibration sequence for a series of ac voltages $V_i^{(ac)}$. (c) Simulated version of the data in (b) using the measured parameters of the device for a series of $\Phi_i^{(ac)}$. (d) Fits of the extracted frequency $\delta\omega$ of the data in (b) to the simulation in (c), assuming a linear relation $V_i^{(ac)} = k(\Phi_i^{(ac)}/\Phi_0)$. The star symbol indicates the typical ac-flux bias point. (e) Measured $\delta\omega$ for $0 < \Delta\theta < 3\pi$ in the presence of adversary ac-flux. The oscillation amplitude (swing of $\delta\omega$) is proportional to the ac-flux crosstalk $\beta^{(ac)}$ as discussed in the main text.

flux bias frequencies. This simulation leads to equivalent Ramsey fringes for a range of $\Phi_i^{(ac)}$; an example is shown in fig. 9(c). We then extracted the frequencies of both the measured and the simulated Ramsey fringes and fitted them to each other by assuming a linear relation, i.e. $V_i^{(ac)} = k_i(\Phi_i^{(ac)}/\Phi_0)$. In our setup, we typically obtain k_i in the range from 6 to 10.

The choice of dc-flux bias points is made by following the typical bias points we use for two-qubit gate operation, which are around $0.3\Phi_0$ [14]. The ac-flux bias point is generally chosen for maximum sensitivity to small changes in ac-flux; an example is shown in fig. 9(c). For the ac-flux frequency, we set $\omega^{(ac)}/2\pi = 200$ MHz, which is a typical frequency for parametric modulation in this system.

Next we assume that the measured ac-flux crosstalk is

small, which allows us to linearise the region around the bias point, i.e. $\Delta\Phi_i^{(ac)} \approx \gamma_i^{(ac)}\Delta(\delta\omega)$. The slope $\gamma_i^{(ac)}$ is extracted using the nearest data points, and it allows us to infer $\Delta\Phi_i^{(ac)}$ from the measured $\Delta(\delta\omega)$: $\beta_{i,j}^{(ac)} = \gamma_i^{(ac)}\Delta(\delta\omega)/2\Phi_j^{(ac)}$.

Appendix C: Qubit frequency allocation

The allocation of qubit frequencies in this processor follows the 2-frequency subgroup strategy as described in Ref. [27] and section II of the main text. Table I shows the target qubit frequency allocation.

Group	Label	f_{01} (GHz)	η (MHz)
A	$\mathbf{a}_1$	4.10	-188
	$\mathbf{a}_2$	3.99	
	$\mathbf{a}_3$	4.17	
	$\mathbf{a}_4$	4.28	
B	$\mathbf{b}_1$	4.75	-229
	$\mathbf{b}_2$	4.70	
	$\mathbf{b}_3$	4.84	
	$\mathbf{b}_4$	4.95	

TABLE I: Qubit frequency allocation. For labels, refer to fig. 2(f) of the main text. f_{01} and η are the qubit frequencies and anharmonicities, respectively.

Appendix D: Measured frequencies

In table II, we list the range of measured or inferred qubit frequencies (f_{01}), anharmonicities (η), readout resonator frequencies (f_r), and coupler frequencies at zero flux bias (f_{c0}). The qubits' and couplers' frequencies are approximately 1 GHz lower than the design values due to an off-target Josephson-junction fabrication result.

Parameters	QPU 1	QPU 2
f_{01} (GHz)	[3.262, 4.077]	[3.166, 3.982]
η (MHz)	[-249, -191]	[-245, -193]
f_r (GHz)	[6.317, 6.987]	[6.335, 7.059]
f_{c0} (GHz)	[6.476, 7.049]	[6.470, 7.329]

TABLE II: Range of measured frequencies of the two QPUs examined in this work.

Appendix E: Complete datasets

Figure 10 shows the complete datasets of measured xy and dc-flux crosstalks from both processors. Due to the different numbers of pairs present in each dataset, we plot a normalised histogram indicated by the normalised count on the vertical axis.

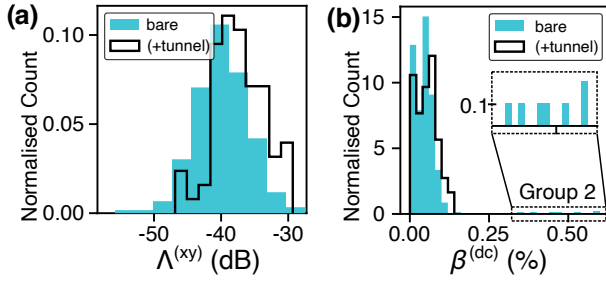


FIG. 10: Complete datasets on the aggregate performance of xy crosstalk $\Lambda^{(xy)}$ and dc-flux crosstalk $\beta^{(dc)}$. (a) Histogram of the on-resonant xy crosstalk $\Lambda_{i,j}$ for a flip-chip module with bare transmission lines (labelled “bare,” 210 pairs, $\bar{\Lambda}_{\text{bare}} = (39.8 \pm 4.0)$ dB), and another flip-chip module with a majority of the transmission lines covered in tunnel structures (labelled “+tunnel,” 72 pairs, $\bar{\Lambda}_{(+\text{tunnel})} = (37.4 \pm 3.9)$ dB). (b) Histogram of the dc-flux crosstalk $\beta^{(dc)}$ (bare: 462 pairs, tunnel: 274 pairs). Data indicated as Group 2 are associated with pairs whose z-lines are nearest neighbour.

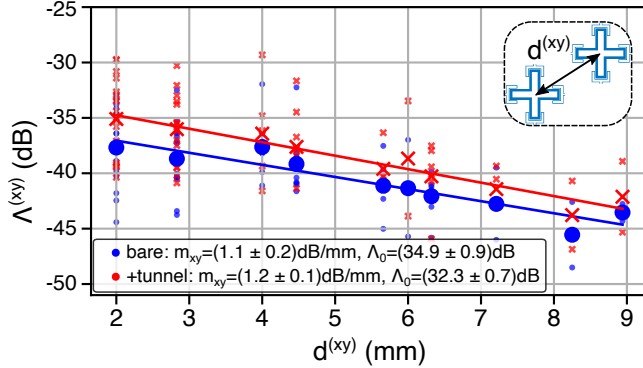


FIG. 11: Data of xy crosstalk $\Lambda^{(xy)}$ vs. the qubit-qubit distance $d^{(xy)}$ with an empirical linear fit.

Appendix F: Empirical linear fit of $\bar{\Lambda}^{(xy)}$ vs $d^{(xy)}$

To further illustrate the trend within the data of average xy crosstalk $\bar{\Lambda}^{(xy)}$ versus the qubit-qubit distance $d^{(xy)}$, we performed an empirical linear fit of the form $\bar{\Lambda}^{(xy)} = m_{xy}d^{(xy)} + \Lambda_0$. The fit is performed by assigning equal weight to each data point. The results are shown in fig. 11. The associated error bars of m_{xy} and Λ_0 are the fit uncertainties. The analyses yield approximately similar m_{xy} and Λ_0 for both processors.

Appendix G: Single-qubit gate error

We introduced the distance-scaling parameters, denoted as m_{xy} and Λ_0 , which are obtained from an empirical linear fit to the data $\bar{\Lambda}^{(xy)}$ vs. $d^{(xy)}$. These parameters can be used as a starting point in estimating the impact of xy crosstalk on the total gate fidelity

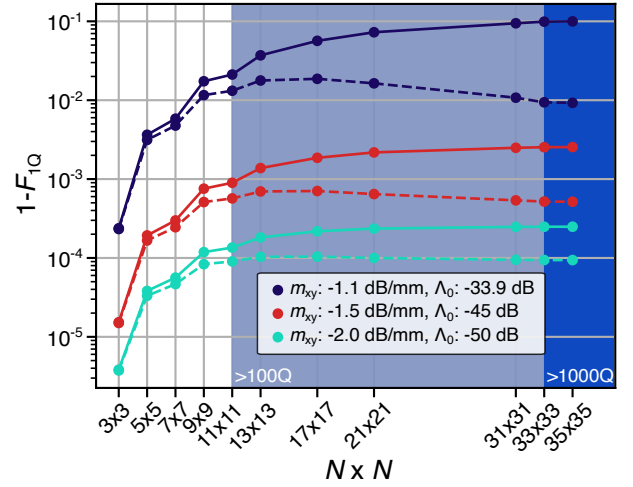


FIG. 12: Predicted total single-qubit gate error in a square lattice of $N \times N$ qubits (nearest-neighbour separation is 2 mm). The gate error is assumed to only come from the off-resonant excitation from adversary single-qubit signals. The solid line represents a scenario described in the text, and the dashed line assumes additional phase related to propagation from the location of the adversary line to the target qubit.

during parallel applications of single-qubit gates. From the hardware-architecture perspective, these parameters should be as low as possible. We find approximately $m_{xy} = -1.1$ dB/mm and $\Lambda_0 = -33.9$ dB.

Clearly, the actual error depends on the pulse sequences (implementing quantum gates) that are being applied to all of the qubits. Here, we consider a specific scenario to obtain a concrete estimate of the effect on gate fidelity: a situation where single-qubit X gates are simultaneously applied on all qubits. The qubit frequencies are allocated according to the two-frequency subgroup strategy shown in fig. 2(f) of the main text and specified in Appendix C. Here, the gate error is due to parasitic excitation (both off-resonant and on-resonant) of the target qubit from adversary X -gates applied to all other xy-lines. These signals are assumed to be on-resonant with the qubits that they are meant to excite. Details on the simulation are described in Appendix H.

The results are shown in fig. 12. The simulation yielding the solid lines assumes no additional phase offset between the signal and the adversary signals. In this case, the total gate error begins to plateau (up to considered processor sizes) as we begin to consider processors with hundreds of qubits, which is attributed to weakening crosstalk due to larger values of $d^{(xy)}$. This assumption of no phase offset is not a realistic one, but we believe it provides an easily understandable setting and a relatively stringent criterion to give us an idea of the total gate error. If we could improve the crosstalk and its scaling behaviour to $m_{xy} = -1.5$ dB/mm and $\Lambda_0 = -45$ dB, for processors with roughly 1000 qubits, we find a projected total single-qubit gate fidelity in excess of 99.7%, and for even better crosstalk, $m_{xy} = -2.0$ dB/mm and

$\Lambda_0 = -50$ dB, we find 99.97 %.

We also simulated the total single-qubit gate error (dashed lines in fig. 12) by assuming additional phase offset due to signal propagation between the positions of the adversary line (approximated as the position of the adversary qubit) and the target qubit. The assumption makes a negligible difference for small qubit arrays due to the small $d^{(xy)}$. The difference is more pronounced for larger qubit arrays, as there are more contributions from target-adversary pairs with larger $d^{(xy)}$. In such a setting, the total gate fidelities for processors beyond 1000 qubits (33×33) increase to 99.95 % for $m_{xy} = -1.5$ dB/mm, $\Lambda_0 = -45$ dB and 99.99 % for $m_{xy} = -2.0$ dB/mm, $\Lambda_0 = -50$ dB.

We emphasize that this is a very simplified model; we have no quantitative model predicting a log-linear behaviour nor that a similar trend would continue beyond the range of d_{xy} examined in this work. However, we believe that these parameters can be useful as a set of quantitative metrics to help guide near-term scaling-up effort and to guide hardware roadmaps.

Appendix H: Numerical simulations

In this section, we briefly describe the models used to numerically simulate the ac-flux calibration curve and the total single-qubit gate error due to xy crosstalk.

1. ac-flux calibration curve

In this simulation, we focus on a system comprising a fixed-frequency qubit coupled to a frequency-tunable coupler. The goal is to extract the Ramsey-fringe frequency of a qubit when the coupler is being subjected to specific dc-flux bias and ac-flux modulation.

The system Hamiltonian $\mathcal{H}_{\text{sys}}$ is

$$\mathcal{H}_{\text{sys}} = \mathcal{H}_q + \mathcal{H}_c + \mathcal{H}_{\text{int}}, \quad (\text{H1})$$

where $\mathcal{H}_q$, $\mathcal{H}_c$, and $\mathcal{H}_{\text{int}}$ represent the Hamiltonian of the qubit, the coupler, and their interaction, respectively. We employ a doubly rotating frame at the qubit-drive angular frequency $\omega^{(xy)}$ and the coupler angular frequency at its dc-flux bias, $\omega_c(\Phi = \Phi^{(\text{dc})})$.

The qubit Hamiltonian is the following

$$\mathcal{H}_q/\hbar = -\Delta_q(\sigma_z \otimes \mathbb{I}) + \Omega^{(xy)}(t)(\sigma_x \otimes \mathbb{I}), \quad (\text{H2})$$

where ω_q is the qubit angular frequency, $\Delta_q = \omega^{(xy)} - \omega_q$, $\Omega^{(xy)}(t)$ is the time-dependent qubit-drive signal appropriately expressed in the angular-frequency unit, and $\sigma_{x/y/z}$ are the Pauli matrices.

The coupler Hamiltonian is

$$\mathcal{H}_c/\hbar = -\Delta_c(t)(\mathbb{I} \otimes \sigma_z), \quad (\text{H3})$$

where $\Delta_c(t) = \omega_c(\Phi^{(\text{dc})}) - \omega_c(\Phi^{(\text{dc})} + \Phi^{(\text{ac})}(t))$, and $\omega_c(\Phi) = \omega_{c0}\sqrt{|\cos(\pi\Phi/\Phi_0)|}$. The parameters ω_{c0} and

Φ_0 are the coupler angular-frequency at zero-flux bias and the magnetic-flux quantum, respectively.

The interaction Hamiltonian is

$$\mathcal{H}_{\text{int}}/\hbar = g e^{i(\omega^{(xy)} - \omega_c(\Phi^{(\text{dc})}))t}(\sigma^+ \otimes \sigma^-) + \text{H.c.}, \quad (\text{H4})$$

where g is the coupler-qubit coupling strength expressed in the angular-frequency unit. Here, we make the rotating-wave approximation to neglect the counter-rotating terms.

We simulate the state of the combined system (both qubit and coupler are initially in the ground state) evolving under $\mathcal{H}_{\text{sys}}$ with the pulse sequence shown in fig. 9(a). The solver is *qutip.sesolve* [56, 57], and the simulation time step is 1 ns. From the expectation value of $\sigma_z \otimes \mathbb{I}$ at the end of the pulse sequence, we reconstruct the expected Ramsey fringes. An example of the simulation result is shown in fig. 9(c).

2. Single-qubit error

In this simulation, consider a system comprising a square array of qubits (total $N \times N$ qubits), each of them being driven by an on-resonant X gate. Due to non-zero xy crosstalk, each qubit also experiences parasitic qubit driving from the rest of the qubits.

We assume distance-dependent xy-crosstalk behaviour that follows the empirical linear model described in Appendix F. We focus on a target qubit at the center of this array (assume N is an odd number). Our goal is to calculate the resultant single-qubit error on this target qubit due to the parasitic drives.

The Hamiltonian of interest considers a single qubit that is being driven by microwave signals. We ignore evolution of other qubits, and group the parasitic drives into the drive term. Specifically,

$$\mathcal{H}_{\text{sys}} = \mathcal{H}_i + \mathcal{H}_{i,j}. \quad (\text{H5})$$

We employ a reference frame rotating with the drive frequency of the target qubit.

The Hamiltonian $\mathcal{H}_i$ is

$$\mathcal{H}_i/\hbar = -\Delta_i\sigma_z + \Omega_{i,i}(t)\sigma_x, \quad (\text{H6})$$

where $\Delta_i = \omega_i^{(xy)} - \omega_i$ is the qubit-drive detuning, assumed to be zero in this simulation. The parameter $\Omega_{i,i}(t)$ is the time-dependent microwave drive pulse amplitude applied to the target qubit by its own xy-line and is appropriately expressed in the angular-frequency unit. The symbols $\sigma_{x/y/z}$ are the Pauli matrices.

The Hamiltonian corresponding to the parasitic drives from other qubits is

$$\mathcal{H}_{i,j}/\hbar = \sum_{j \neq i} \Omega_{i,j}(t)(\sigma_x \cos(\phi_j(t)) + \sigma_y \sin(\phi_j(t))), \quad (\text{H7})$$

where $\phi_j(t) = \delta_{i,j}t + \phi_{i,j}$. The parameters $\delta_{i,j}$ and $\phi_{i,j}$ are the detuning ($\omega_j - \omega_i$) and the additional phase, respectively. For simplicity, each qubit drive is assumed to produce the same Rabi angular frequency to its own qubit. Thus $\Omega_{i,i}(t) = \Omega^{(xy)}(t)$ for any i . The parasitic Rabi amplitude $\Omega_{i,j}$ is

$$\Omega_{i,j}(t) = 10^{\Lambda_{i,j}/20} \Omega^{(xy)}(t), \quad (\text{H8})$$

where $\Lambda_{i,j} = m_{xy}d_{i,j} + \Lambda_0$, and $d_{i,j}$ is the distance between q_i and q_j . The phase $\phi_{i,j}$ is the phase related to crosstalk between the adversary xy -line xy_j and the tar-

get qubit q_i . In fig. 12, we simulated two specific cases: $\phi_{i,j} = 0$ (solid line), and $\phi_{i,j} = (\omega_j/c)d_{i,j}$ (dashed line) corresponding to the phase delay due to signal propagation from the location of the adversary qubit to the location of the target qubit, through vacuum.

We employ *qutip.sesolve* solver [56, 57], with a simulation time step of 0.125 ns. From the expectation value of σ_z , we extract the probability P_g of the qubit being in the ground state at the end of the pulse sequence. We repeat this simulation for a target qubit with the eight different frequencies in Appendix C, and we average the probabilities. This is the single-qubit gate error ($1 - F_{1Q}$) that is plotted on the vertical axis of fig. 12.

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