Solid-State Electrochemical Thermal Transistors with Large Thermal Conductivity Switching Widths

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Thermal transistors that switch the thermal conductivity (κ) of the active layers are attracting increasing attention as thermal management devices. For electrochemical thermal transistors, several transition metal oxides (TMOs) have been proposed as active layers. After electrochemical redox treatment, the crystal structure of the TMO is modulated, which results in the κ switching. However, the κ switching width is still small (< 4 W m⁻¹ K⁻¹). In this study, we demonstrate that LaNiO_x-based solid-state electrochemical thermal transistors have a κ switching width of 4.3 W m⁻¹ K⁻¹. Fully oxidised LaNiO₃ (on state) has a κ of 6.0 W m⁻¹ K⁻¹ due to the large contribution of electron thermal conductivity (κ_{ele} , 3.1 W m⁻¹ K⁻¹). In contrast, reduced LaNiO_{2.72} (off state) has a κ of 1.7 W m⁻¹ K⁻¹ because the phonons are scattered by the oxygen vacancies. The LaNiO_x-based electrochemical thermal transistor exhibits excellent cyclability of κ and the crystalline lattice of LaNiO_x. This electrochemical

thermal transistor may be a promising platform for next-generation devices such as thermal displays.

1. Introduction

Reuse of waste heat resulting from the low conversion rate of primary energy is crucial for sustainable development. Low- to medium-temperature (100–300 °C) waste heat is the most difficult to reuse; the temperature is too low to generate jet steam for power generation. Although thermoelectric energy conversion technology is a solution, its efficiency is too low in this temperature range in air^[1-4]. Thermal management technologies^[5] such as thermal diodes^[6-8] and thermal transistors^[9-16] have recently attracted attention. Thermal diodes rectify the heat flow; thermal transistors electrically switch the heat flow on and off. We expect that thermal displays that visualise heat contrast using infrared cameras can be realised using thermal transistors. Thus, thermal transistors may be useful for reuse of waste heat.

For this purpose, electrical control of thermal conductivity (κ) in the active materials of thermal transistors is paramount. It necessitates a switch between the on state (high κ) and off state (low κ). Electrochemical^[10-14] and electrostatic^[15, 16] approaches offer pathways to govern the κ of active materials. Although electrostatic methods provide rapid κ control, their suitability for thermal display applications is limited by the requirement of an extremely thin active material around the heterointerface between the gate dielectric and the active material. We focus on electrochemical methods because they control the κ of entire materials. Many studies have used ionic liquids such as organic electrolytes and water for electrochemical modulation of materials^[10-12, 14]. However, this method is incompatible with integrated circuits, limiting its application. In our pursuit of thermal displays with substantial thermal conductance differences between the on and off states, we used all-solid-state electrochemical thermal transistors^[13, 17, 18].

All-solid-state electrochemical thermal transistors, a cornerstone of advanced thermal management, harness the redox modulation of transition metal oxides (TMOs). Among many candidates^[9-16], TMOs have emerged as promising materials. When subjected to electrochemical redox treatment by inserting and extracting metal ions^[10] and oxide ions^[12-14], TMOs undergo structural transformations leading to a switch in their κ width. Despite these advancements, the challenge lies in achieving a substantial κ switching width, a critical factor for practical application that is often limited (< 4 W m⁻¹ K⁻¹)^[10, 12-14, 19].

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To overcome this limitation, we chose LaNiO₃ as the active material for solid-state electrochemical thermal transistors. Bulk LaNiO₃ has comparably high electrical and thermal conductivity^[20], indicating its potential for thermal conductivity modulation (**Supplementary Information S1**). The schematic depicted in **Fig. 1** introduces LaNiO_x as the active layer, offering a wide κ switching width. In the on state, LaNiO₃ has heightened electrical conductivity when fully oxidised, resulting in a significant contribution from the electron thermal conductivity. Conversely, the off state achieved through electrochemical reduction leads to oxygen vacancies, reduced electrical conductivity, and negligible electron thermal conductivity. Scattering of phonons by these vacancies manifests as a low thermal conductivity.

This study focuses on use of LaNiO_x-based electrochemical thermal transistors to address the limitations in κ switching width. Our investigations indicated a κ switching width of 4.3 W m⁻¹ K⁻¹. Fully oxidised LaNiO₃ (on state) exhibited a high κ of 6.0 W m⁻¹ K⁻¹, primarily attributed to the contribution of electron thermal conductivity (3.1 W m⁻¹ K⁻¹). Conversely, reduced LaNiO_{2.72} (off state) had a low κ of 1.7 W m⁻¹ K⁻¹ due to scattering of phonons by oxygen vacancies. Both the reduction and oxidation processes exhibited a nearly linear change in thermal conductivity.

Furthermore, our study investigates the cyclability of κ and the crystalline lattice of LaNiO_xbased thermal transistors. The exceptional performance of these electrochemical thermal transistors positions them as viable candidates for integration into next-generation devices, particularly thermal displays.

2. Results and Discussion

2.1. Electrochemical Thermal Transistor Fabrication and Operation

Figure 2a shows a schematic of the thermal transistor device structure, which is similar to those of our previous thermal transistors^[13, 17, 18]. In this study, we inserted an extremely thin $SrCoO_x$ layer between the LaNiO₃ and solid electrolyte (Gd-doped CeO₂/YSZ)

(Supplementary Information S2). As shown in Supplementary Fig. S2, when LaNiO₃ was grown on the $SrCoO_x/GDC$ -buffered (001) YSZ, the crystallographic orientation was stronger than that without a buffer layer. X-ray reciprocal space mapping (RSM) around 113 YSZ diffraction spots (data not shown) confirmed that LaNiO₃ grown on $SrCoO_x/GDC$ -buffered

(001) YSZ demonstrated the highest quality. Moreover, there was a positive correlation between the quality of LaNiO₃ and its thermal conductivity (**Supplementary Table S3**). Thus, use of the thermal transistor structure shown in **Fig. 2a** is crucial.

The setup for operation of the LaNiO_x thermal transistor is shown in **Fig. 2b**. Electrochemical redox treatment was performed at 280 °C in air by applying a constant current of ±10 μ A. During the redox reaction, we controlled the flown electron density $Q = (I \cdot t)/(e \cdot V)$ through the current application time (**Figs. 2c and 2d**), with a step of $Q = 2 \times 10^{21}$ cm⁻³ marked as A – K, where *I* is the flown current, *t* is the application time, *e* is the electron charge, and *V* is the volume of the LaNiO_x layer in the thermal transistor. In this study, electrochemical redox treatments were performed according to Faraday's law of electrolysis.

Reduction: $LaNiO_3 + 0.56e^- \rightarrow LaNiO_{2.72} + 0.28O^{2-}$

Oxidation: $LaNiO_{2.72} + 0.28O^{2-} \rightarrow LaNiO_3 + 0.56e^{-}$

The conductivity of the reduced state of LaNiO_{2.72} (9 S cm⁻¹) also confirmed its identity as LaNiO_{2.72}^[21].

Electrochemical redox treatment was initiated by applying a negative current to reduce LaNiO₃ to LaNiO_{2.72} (**Fig. 2c**). As *Q* increased, the absolute value of the voltage increased. The slope decreased after 2×10^{21} cm⁻³ and slightly increased after 2×10^{21} cm⁻³. When the current became positive, LaNiO_{2.72} was oxidised to LaNiO₃ (**Fig. 2d**). As *Q* increased, fluctuations occurred at 2×10^{21} cm⁻³ and 8×10^{21} cm⁻³. Overall, there was still an increasing trend and an absolute value between 3 V and 5 V, with minimal variations. The absence of steps in the process curve indicates that there were no new thermodynamically stable phases.

2.2. Crystalline Lattice and Thermal Conductivity Changes during Redox Treatment

Redox treatment induced reversible changes in the crystalline lattice of LaNiO_x step by step (reduction $A \rightarrow F$, oxidation: $F \rightarrow K$), as evidenced by the out-of-plane x-ray diffraction patterns (**Fig. 3a**). Slight shifts in the 002 diffraction peak indicated modulations in the crystal structure, with lattice expansion observed after reduction and shrinkage observed after oxidation. The change in the lattice parameter *c* is shown in **Fig. 3b**.

Figure 4 and Supplementary Fig. S3 illustrate the significant changes in the κ of the LaNiO_x during redox treatment. Time-domain thermoreflectance (TDTR) decay curves show a decrease in κ from 5.9 W m⁻¹ K⁻¹ to 1.8 W m⁻¹ K⁻¹ after reduction (A \rightarrow F) and an increase

from 1.8 W m⁻¹ K⁻¹ to 5.9 W m⁻¹ K⁻¹ after oxidation (F \rightarrow K). Both the reduction and oxidation processes exhibited a nearly linear change in thermal conductivity. The slight variations in lattice constants between the oxidised and reduced states are attributed to the disappearance and generation of oxygen vacancies. Through phonon scattering, oxygen vacancies contribute to a decrease in the lattice thermal conductivity.

However, there is a significant contrast in electrical conductivity (σ) between the oxidised (4250 S cm⁻¹) and reduced (9 S cm⁻¹) states (**Supplementary Table S4**). We estimated the electron thermal conductivity (κ_{ele}) by assuming the Wiedemann–Franz law; $\kappa_{ele} = L \cdot \sigma \cdot T$, where *L* is the Lorentz number (2.44 × 10⁻⁸ W Ω K⁻²), and *T* is the absolute temperature. The κ_{ele} of the oxidised state reached 3.1 W m⁻¹ K⁻¹. According to the principle that observable thermal conductivity is the sum of lattice thermal conductivity (κ_{lat}) and $\kappa_{ele}^{[22]}$, we estimated the κ_{lat} of LaNiO₃ (on state) to be 2.9 W m⁻¹ K⁻¹. This value aligns with previously reported values for bulk LaNiO₃^[20], confirming the consistency of our findings. This substantial difference enabled the LaNiO_x thermal transistor to modulate its thermal conductivity indicate the potential of the LaNiO_x-based thermal transistor for precise thermal modulation.

2.3. Cycle Properties of Thermal Transistor

As shown in **Fig. 5 and Supplementary Fig. S4**, the LaNiO_x-based thermal transistor exhibits exceptional cycling properties. The on state (LaNiO₃) has a higher average thermal conductivity (6.0 W m⁻¹ K⁻¹) than the off state (LaNiO_{2.72}, 1.7 W m⁻¹ K⁻¹). Seven cycles are shown in the figure. The TDTR decay of LaNiO₃ was faster than that of LaNiO_{2.72} (**Fig. 5a**). The TDTR curves for each cycle overlapped significantly, indicating excellent repeatability.

2.4. Comparison with Other TMO Thermal Transistors

Figure 6 compares the thermal conductivity switching widths of different TMOs, indicating the unparalleled performance of LaNiO_x-based thermal transistors, with a thermal conductivity switching width of approximately 4.3 W m⁻¹ K⁻¹, significantly greater than that of other TMOs. The wide switching range indicates the exceptional versatility of LaNiO_x in modulating its thermal conductivity. The inherent ability of LaNiO_x-based thermal transistors to linearly transition between high thermal conductivity in the fully oxidised state and low thermal conductivity in the reduced state positions them at the forefront of TMOs for thermal management applications. The nuanced control over thermal conductivity and the stability

demonstrated in the cycling properties (**Fig. 5**) underscore the potential of $LaNiO_x$ -based thermal transistors for application in next-generation thermal displays and other advanced thermal management systems.

3. Conclusion

This study presents a breakthrough with LaNiO_x-based electrochemical thermal transistors, with an exceptional κ switching width of 4.3 W m⁻¹ K⁻¹. The fully oxidised LaNiO₃ (on state) produced a κ of 6.0 W m⁻¹ K⁻¹, primarily attributed to a substantial contribution from electron thermal conductivity (3.1 W m⁻¹ K⁻¹). In contrast, the reduced LaNiO_{2.72} (off state) had a low κ of 1.7 W m⁻¹ K⁻¹ due to negligible electron thermal conductivity (0.007 W m⁻¹ K⁻¹) and phonon scattering caused by oxygen vacancies. The LaNiO_x-based electrochemical thermal transistor demonstrated outstanding κ cyclability while maintaining the structural integrity of the LaNiO_x crystalline lattice, making it a promising candidate for integration into next-generation devices, particularly thermal displays.

4. Experimental Section

Fabrication of thermal transistors: LaNiO₃ films were heteroepitaxially grown on SrCoO_x/10%-Gd-doped CeO₂ (GDC)-buffered (001)-oriented YSZ substrates using pulsed laser deposition (PLD). First, approximately10-nm-thick GDC was heteroepitaxially grown on a YSZ (10 mm × 10 mm × 0.5 mm, double-sided polished, crystal base) substrate at 770 °C in an oxygen atmosphere (10 Pa). Approximately 2-nm-thick SrCoO_x was grown on GDC in the same conditions. Focused KrF excimer laser pulses ($\lambda = 248$ nm, fluence ~2 J cm⁻² pulse⁻¹, repetition rate = 10 Hz) were irradiated onto the ceramic target of GDC. Subsequently, an approximately 80-nm-thick LaNiO₃ film was heteroepitaxially grown on the GDC film at 625 °C in an oxygen atmosphere (25 Pa). The laser fluence was approximately 1.6 J cm⁻² pulse⁻¹. After film growth, the sample was cooled to room temperature in a PLD chamber in an oxygen atmosphere (25 Pa). An approximately 50-nm-thick Pt film was sputtered on the top surface of the LaNiO₃ epitaxial film, followed by an approximately 50nm-thick Pt film sputtered on the backside of the YSZ substrate. Pt sputtering was performed at room temperature. The samples were cut into four squares (5 mm × 5 mm).

Electrochemical redox treatment: thermal transistor (5 mm \times 5 mm) was placed on a Ptcoated glass substrate and heated at 280 °C in air. Electrochemical redox treatment was performed by applying a constant current of $\pm 10 \ \mu$ A, after which the sample was immediately cooled to room temperature.

Crystallographic analyses: The crystalline phase, orientation, and lattice parameters of the resultant films were analysed using high-resolution x-ray diffraction (Cu K α_1 , $\lambda = 1.54059$ Å, ATX-G, Rigaku). Out-of-plane Bragg diffraction patterns and reciprocal space mappings (RSMs) were measured at room temperature to clarify changes in the crystalline phase of LaNiO_x. The lattice parameters were calculated from the diffraction peaks. The atomic arrangements of the LaNiO₃ films were visualised using a STEM (JEM-ARM200CF, JEOL) operated at 200 keV.

Measurement of electrical properties of LaNiO_x layers: To measure the electrical conductivity (σ) of the LaNiO_x layers after redox treatment, we mechanically attached Au foil on the film surface while Pt films were deposited only on the backside of the YSZ substrate^[13]. The LaNiO_x films were oxidised and reduced electrochemically at 280 °C in air using the Au foil as the electrode. The σ of the LaNiO₃ (on state) and LaNiO_{2.72} (off state) films was measured using the DC four-probe method with a van der Pauw electrode configuration at room temperature in air.

Thermal conductivity measurements: The κ of the LaNiO₃ layers perpendicular to the substrate surface was measured through time-domain thermoreflectance (TDTR, PicoTR, PicoTherm). The top Pt film was used as the transducer. The decay curves of the TDTR signals were simulated to obtain κ . The specific heat capacities of the layers used for the TDTR simulation were Pt: 132 J kg⁻¹ K⁻¹ [²³]; LaNiO₃: 448 J kg⁻¹ K⁻¹ [²⁴], and YSZ: 460 J kg⁻¹ K⁻¹ [²⁵]. Details of the TDTR method are described in our previous studies^[13, 17, 26-28]. In treatment of the thermal conductivity values, as there were uncertainties such as the position of the baseline, position of time zero, and noise in the signal, we used error bars for ±15% of the obtained values.

Acknowledgements

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Figure 1. Strategy of electrochemical thermal transistors with transition metal oxide active layer with large thermal conductivity switching width. (Left) Diagram of on state. Fully oxidised TMOs show high electrical conductivity. Both electrons and phonons carry heat. The thermal transistor shows high thermal conductivity. (Right) Diagram of off state. Electrochemical reduction treatment produces oxygen vacancies. The reduced TMOs show low electrical conductivity. The electron thermal conductivity is negligible. Phonons are scattered by oxygen vacancies. The thermal transistor shows low thermal conductivity.



Figure 2. LaNiO_x-based thermal transistor operation. (a) Structure of thermal transistor composed of six layers: 50-nm-thick Pt film, 80-nm-thick LaNiO_x film, 2-nm-thick SrCoO_x film, 10-nm-thick Gd-doped CeO₂ (GDC) film, 0.5-mm-thick (001) YSZ single-crystal substrate, and 40-nm-thick Pt film. (b) Schematic of LaNiO_x thermal transistor. The transistor was placed on a Pt-coated glass substrate and heated at 280 °C in air. A K-type thermocouple was used to monitor the transistor surface temperature. The transistor measured 5 mm × 5 mm. A constant negative current (-10μ A) was applied for reduction; a constant positive current ($+10 \mu$ A) was applied for oxidation. (c)(d) Changes in observed DC voltage of thermal transistor during (c) reduction from LaNiO₃ to LaNiO_{2.72} and (d) oxidation from LaNiO_{2.72} to LaNiO₃ with a step of $Q = 2 \times 10^{21}$ cm⁻³.



Figure 3. Change in crystalline lattice of LaNiO_x layer after redox treatment. (a) Change in out-of-plane XRD patterns after redox treatment with a step of $Q = 2 \times 10^{21}$ cm⁻³. The 002 diffraction peak shifted to a smaller q_z side after reduction and a larger q_z side after oxidation. These shifts were entirely reversible. (b) Changes in lattice parameter *c* of LaNiO_x as a function of *Q*. A lattice expansion of approximately 0.6% occurred after reduction.



Figure 4. Change in thermal conductivity (κ) of LaNiO_x layer after redox treatment. (a) TDTR decay curves of thermal transistor after (upper) reduction and (lower) oxidation treatment. (b) Changes in thermal conductivity of LaNiO_x layer after (left) reduction and (right) oxidation treatment with a step of $Q = 2 \times 10^{21}$ cm⁻³. The κ of LaNiO₃ was 5.9 W m⁻¹ K⁻¹; it decreased almost linearly with Q after reduction. After oxidation, the κ increased almost linearly with Q and returned to 5.9 W m⁻¹ K⁻¹.



Figure 5. Cycle properties of LaNiO_x-based thermal transistor. (a) Changes in TDTR decay curves (seven cycles overlapped). The TDTR decay of the LaNiO₃ layer was faster than that of the LaNiO_{2.72} layer. (b) Change in thermal conductivities of LaNiO₃ and LaNiO_{2.72} layers after redox cycling. The average thermal conductivities of the LaNiO₃ (on state) layer and LaNiO_{2.72} (off state) layer were 6.0 W m⁻¹ K⁻¹ and 1.7 W m⁻¹ K⁻¹, respectively. The electron thermal conductivity of the LaNiO₃ (on state) layer was high (3.1 W m⁻¹ K⁻¹). The electron thermal conductivity of the LaNiO_{2.72} (off state) layer was negligible.



Figure 6. Comparison of thermal conductivity switching widths of several transition metal oxides. LaNiO_x-based thermal transistors exhibited large thermal conductivity switching widths (~4.3 W m⁻¹ K⁻¹). Data for LiCoO₂ \leftrightarrow Li_{1- δ}CoO₂ are from Ref. 10^[10], SrCoO₃ \leftrightarrow SrCoO_{2.5} and SrCoO_{2.5} \leftrightarrow HSrCoO_{2.5} are from Ref. 12^[12], SrCoO₃ \leftrightarrow SrCoO₂ are from Ref. 13^[13], WO₃ \leftrightarrow H_{δ}WO₃ are from Ref. 19^[19], and La_{0.5}Sr_{0.5}CoO₃ (LSCO₃) \leftrightarrow La_{0.5}Sr_{0.5}CoO_{2.5} (LSCO_{2.5}) are from Ref. 14^[14].

The table of contents entry should be 50–60 words long and should be written in the present tense. The text should be different from the abstract text.

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Supporting Information

Solid-State Electrochemical Thermal Transistors with Large Thermal Conductivity Switching Widths

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S1: Selection of LaNiO₃ as the active layer (Table S1, Table S2, Figure S1)

S2. Fabrication of LaNiO₃-based solid-state thermal transistors (Figure S2, Table S3, Table S4)

S3. Repeated thermal conductivity measurements of LaNiO₃-based solid-state thermal transistors (Figure S3, Figure S4)

S1. Selection of LaNiO₃ as the active layer

In this study, we focused on perovskite-structured *Ln*NiO₃ (*Ln* = La, Nd, and Sm) as the active layer for the solid-state electrochemical thermal transistor. **Table S1** summarizes the electrical conductivity (σ) and the thermal conductivity (κ) of bulk *Ln*NiO₃ (*Ln* = La, Nd, and Sm) at room temperature^[20]. At room temperature, bulk *Ln*NiO₃ (*Ln* = La, Nd, and Sm) shows the following κ ; LaNiO₃: 10.7 W m⁻¹ K⁻¹, NdNiO₃: 6.5 W m⁻¹ K⁻¹, and SmNiO₃: 4.0 W m⁻¹ K⁻¹. Thus, LaNiO₃ is a promising candidate as the active layer of the thermal transistors. It should be noted that the σ of LaNiO₃ is 10500 S cm⁻¹. We assumed the Wiedemann-Frantz law for the estimation of electron contribution to the observed thermal conductivity ($\kappa_{ele} = L \cdot \sigma \cdot T$, where *L* is the Lorentz number of 2.44 × 10⁻⁸ W Ω K⁻² and *T* is the absolute temperature of 298 K) and obtained κ_{ele} of 7.6 W m⁻¹ K⁻¹.

Table S1. The electrical conductivity (σ) and the thermal conductivity (κ) of bulk *Ln*NiO₃ (*Ln* = La, Nd, and Sm) at room temperature. The ionic radius data is from Shannon's report.^[2]

JS. Zhou et al., PRB 67, 020404(R) (2003) ^[1]	LaNiO ₃	NdNiO ₃	SmNiO ₃
Ionic radius of Ln^{3+} ion (Å) (C.N. = 12)	1.36	1.27	1.24
Electrical conductivity at RT (S cm ⁻¹)	10500	3400	
Total thermal conductivity, κ (W m ⁻¹ K ⁻¹)	10.7	6.5	4.0
Electron thermal conductivity, κ_{ele} (W m ⁻¹ K ⁻¹)	7.6	2.5	0
Lattice thermal conductivity, κ_{lat} (W m ⁻¹ K ⁻¹)	3.1	4.0	4.0

To check the potential of LaNiO₃ epitaxial films as the active layer of the thermal transistors, we fabricated LaNiO₃ epitaxial films on (001) SrTiO₃ substrates and measured the electrical and thermal conductivity of the resultant films at room temperature (**Table S2**). The σ of the resultant LaNiO₃ film was only 135 S cm⁻¹, two orders of magnitude smaller than that of bulk. The κ in the out-of-plane of the LaNiO₃ film was 7.3 W m⁻¹ K⁻¹. If we assumed the Wiedemann-Frantz law for the estimation of κ_{ele} , the κ_{ele} of the LaNiO₃ film was only 0.1 W m⁻¹ K⁻¹, reflecting the κ_{lat} of LaNiO₃ is 7.2 W m⁻¹ K⁻¹.

Table S2. The electrical and thermal conductivity of the LaNiO₃ epitaxial films on (001) SrTiO₃ at room temperature.

This study	LaNiO ₃
Ionic radius of Ln^{3+} ion (Å) (C.N. = 12)	1.36
Electrical conductivity at RT (S cm ⁻¹)	135
Total thermal conductivity, κ (W m ⁻¹ K ⁻¹)	7.3
Electron thermal conductivity, κ_{ele} (W m ⁻¹ K ⁻¹)	0.1
Lattice thermal conductivity, κ_{lat} (W m ⁻¹ K ⁻¹)	7.2

Since the estimated κ_{lat} of the LaNiO₃ film on (001) SrTiO₃ substrate is higher than that of the bulk, there is a possibility that we underestimated the κ_{ele} of the LaNiO₃ film. To clarify the origin of it, we observed the microstructure using Cs-corrected scanning transmission electron

microscopy (**Fig. S1**). The columnar structure is visualized in the LaNiO₃ film (**Fig. S1a**). The magnified image (**Fig. S1b**) reveals that there are many planer defects due to the formation of Ruddlesden-Popper phases. Since the electron transport is suppressed by the planer defects, the observed electrical conductivity in the in-plane direction would be lower than that in the out-of-plane direction.



Figure S1. Microstructure of the LaNiO₃ **film grown on (001) SrTiO**₃ **substrate. a,** Low magnification cross-sectional HAADF-STEM image. Stripe patterns (yellow arrows) indicates that columnar growth of LaNiO₃ occurred. **b,** Lattice image around the LaNiO₃/SrTO₃ heterointerface. Planar defects (green arrows) are visualized.

S2. Fabrication of LaNiO₃-based solid-state thermal transistors

Firstly, we fabricated LaNiO₃ films directly on (001) YSZ substrates. **Figure S2a** shows the out-of-plane XRD pattern of the resultant film. Together with 001 and 002 diffraction peaks of LaNiO₃, 110 diffraction peaks of LaNiO₃ are seen with 002 YSZ, indicating the mixed orientation of the film. The out-of-plane rocking curve of the 002 LaNiO₃ (**Fig. S2d**) is broad (the full width at half maximum, FWHM ~3.1°). Then, we fabricated LaNiO₃ films on GDC-buffered (001) YSZ substrates. As shown in **Fig. S2b**, intense diffraction peaks of 001 and 002 LaNiO₃ are seen together with 002 GDC and 002 YSZ. The FWHM of the 002 LaNiO₃ is 1.6° as shown in **Fig. 2e**. The reciprocal space mapping (RSM, not shown) of the film revealed that the LaNiO₃ is heteroepitaxially grown on the GDC-buffered YSZ substrate. To further improve the crystallographic orientation of the film, we inserted thin (~2 nm) SrCoO_x layer between the LaNiO₃ and GDC-buffered substrate. The out-of-plane XRD peaks became stronger (**Fig. S2c**) and the tilting became small (1.2°) as shown in **Fig. S2f**.



Figure S2. XRD patterns of the LaNiO³ **films grown on various substrates. a, b, c,** Outof-plane Bragg diffraction patterns of the LaNiO₃ films grown on (a) bare (001) YSZ substrate, (b) GDC-buffered (001) YSZ substrate, and (c) SrCoO_x/GDC-buffered (001) YSZ substrate. **d, e, f,** Out-of-plane rocking curves of 002 LaNiO₃ of the films on (d) bare (001) YSZ substrate, (e) GDC-buffered (001) YSZ substrate, and (f) SrCoO_x/GDC-buffered (001) YSZ substrate.

Then, we measured the σ and the κ of the resultant LaNiO₃ films on the various substrates at room temperature. **Table S3** summarizes the results. The LaNiO₃ film on the SrCoO_x-buffered substrate showed the highest σ of 4200 S cm⁻¹, reflecting the improvement of the crystallographic orientation of the LaNiO₃ film. The out-of-plane κ of the LaNiO₃ film on the SrCoO_x-buffered substrate was the highest (5.7 W m⁻¹ K⁻¹) among the films on different three substrates. We estimated the κ_{ele} and the κ_{lat} of the LaNiO₃ films. The κ_{lat} of the LaNiO₃ film on SrCoO_x-buffered substrate was 2.7 W m⁻¹ K⁻¹, similar to that of bulk (3.1 W m⁻¹ K⁻¹).

Table S3. Electrical and thermal conductivity of the LaNiO₃ films grown on the three different substrates.

	Bare YSZ	GDC-	SCO-
		buffered	buffered
Electrical conductivity, σ (S cm ⁻¹)	500	1200	4200
Thermal conductivity, κ (W m ⁻¹ K ⁻¹)	1.6	4	5.7
Electron thermal conductivity, κ_{ele} (W m ⁻¹ K ⁻¹)	0.36	0.88	3.0
Lattice thermal conductivity, κ_{lat} (W m ⁻¹ K ⁻¹)	1.2	3.1	2.7

Then, we reduced the LaNiO₃ film on SCO-buffered (001) YSZ substrate electrochemically, and measured the σ and the κ (**Table S4**). The reduction treatment by applying total Q of 1×10^{22} cm⁻³ results in the significant reduction of both σ and the κ .

Table S4. Electrical and thermal conductivity of the LaNiO₃ films on SrCoO_x/GDCbuffered substrate (oxidized state and reduced state).

	Oxidized	Reduced
Electrical conductivity, σ (S cm ⁻¹)	4200	9
Thermal conductivity, κ (W m ⁻¹ K ⁻¹)	5.9	1.8
Electron thermal conductivity, κ_{ele} (W m ⁻¹ K ⁻¹)	3.1	0.006
Lattice thermal conductivity, κ_{lat} (W m ⁻¹ K ⁻¹)	2.8	1.8

S3. Repeated thermal conductivity measurements of the LaNiO₃-based solid-state thermal transistors



Figure S3. Change in the thermal conductivity of the LaNiO₃ layer in the thermal transistor. a, b, TDTR phase signal decay curves during (a) reduction and (b) oxidation. The reduction treatment was performed in the order of A, B, C,...F with a step of $Q = 2 \times 10^{21}$ cm⁻³. The oxidation treatment was performed in the order of F, G, H,...K with a step of $Q = 2 \times 10^{21}$ cm⁻³.



Figure S4. TDTR decay cycle of the LaNiO₃ **layer in the thermal transistor. a, b,** TDTR phase signal decay curves after (a) reduction and (b) oxidation.

References

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