

Towards scalable cryogenic quantum dot biasing using memristor-based DC sources

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Abstract—Cryogenic memristor-based DC sources offer a promising avenue for in situ biasing of quantum dot arrays. In this study, we present experimental results and discuss the scaling potential for such DC sources. We first demonstrate the operation of a commercial discrete operational amplifier down to 1.2 K which is used on the DC source prototype. Then, the tunability of the memristor-based DC source is validated by performing several 250 mV-DC sweeps with a resolution of 10 mV at room temperature and at 1.2 K. Additionally, the DC source prototype exhibits a limited output drift of $\approx 1 \mu\text{V s}^{-1}$ at 1.2 K. This showcases the potential of memristor-based DC sources for quantum dot biasing. Limitations in power consumption and voltage resolution using discrete components highlight the need for a fully integrated and scalable complementary metal-oxide-semiconductor-based (CMOS-based) approach. To address this, we propose to monolithically co-integrate emerging non-volatile memories (eNVMs) and 65 nm CMOS circuitry. Simulations reveal a reduction in power consumption, down to 10 μW per DC source and in footprint. This allows for the integration of up to one million eNVM-based DC sources at the 4.2 K stage of a dilution fridge, paving the way for near term large-scale quantum computing applications.

Index Terms—Memristors, Cryogenic electronics, Quantum dots (QDs)

I. INTRODUCTION

QUANTUM computing promises breakthrough applications in a variety of fields, including chemistry [1], finance [2] and climate [3]. Several physical platforms have been proposed to realize quantum computers, ranging from superconducting circuits [4], [5] to trapped ions [6], [7]. Among these candidates, silicon quantum dots (QDs) benefit from a nanometric qubit pitch [8], a long coherence time [9] compared to traditional superconducting qubits, and a temperature of operation up to 4.2 K [10]–[12]. Additionally, QDs appear to be a highly scalable technology thanks to their compatibility with industrial semiconductor fabrication processes [13], [14], demonstrating their potential for industrial-scale production and monolithic co-integration with control electronics [15]. Yet, millions of physical qubits compatible with quantum error correction protocols will be required to unlock these promised applications [16]. Recently, notable advancements have been made, such as enhancements in gate fidelity [17], early scalable QDs matrices [18], [19], and large-scale fabrication of qubits [20], [21]. While these developments contribute to scaling to millions of physical qubits, the linear approach used to control

these QDs emerges as a bottleneck, impeding the seamless integration of an increasing number of qubits. To address this challenge, concurrent scaling of control electronics becomes imperative to ensure the scalability of the QD control method. Early scaling propositions have explored the avenue of cryo-complementary metal-oxide-semiconductor (cryo-CMOS) technology [22], [23]. In particular, mixed-signal solutions have emerged as a principal focus to perform state manipulation and readouts with cryogenic digital-to-analog converters (DACs) to generate pulses [24], [25], cryogenic flip-flop memory to store measurement protocols [26], and amplifier/mixer circuits [27]. Cryogenic DACs with monolithically integrated switched-capacitors have also been proposed to perform in situ biasing of QD gates [15], [28]. The required biasing voltages of the QDs are stored in the charge of the capacitors conceptually close to dynamic random access memories (DRAMs) [26]. This approach benefits from ultra-low power dissipation in the few tens of picowatts but requires periodical refreshment of the capacitor charge due to leakage current, approximately every 10 μs –1 ms [26], [28], to maintain the integrity of the biasing voltage. To avoid this volatility, which will be problematic when scaling up QD-based systems, a memristor-based biasing circuit has been proposed. This circuit exploits the non-volatility of TiO_x memristors at the cost of power dissipation on the order of a few milliwatts [29], which could be reduced to tens of microwatts by using integrated circuits. The behavior of TiO_x -based memristors has been widely studied at cryogenic temperatures, demonstrating DC resistive switchings [30], [31] and analog programming with up to 4-bit memristors [29], [32]. However, the concept of memristor-based DC sources is yet to be experimentally demonstrated at cryogenic temperatures.

In this paper, we investigate the cryogenic DC behavior of a transimpedance amplifier (TIA) based on a commercial operational amplifier (OpAmp) AD8605 between 1.2 K and 300 K. We then propose a prototype of a memristor-based DC source using the cryo-compatible AD8605 OpAmp. This circuit is characterized at 1.2 K and at room temperature which serves as a performance benchmark. We perform DC sweeps with a voltage range of 250 mV and a 10 mV resolution. Additionally, we study the stability of the output voltage ensuring that it does not change over time due to memristor

resistance drift. Finally, we discuss the scalability of this prototype and propose an alternative design to reduce the overall power consumption and footprint. This architecture supposes near-perfect memristors co-integrated with 65 nm CMOS technology to bias the gates of a silicon quantum dot cooled to 4.2 K.

II. MEMRISTOR-BASED DC SOURCE PROTOTYPE

Earlier work conceptualized a memristor-based DC source compatible with cryogenic temperatures [29]. This concept uses a single OpAmp placed in a TIA circuit configuration. The resistive feedback of the TIA is achieved using either a single memristor or multiple memristors in parallel placed in the feedback loop of the OpAmp (see Fig. 1). The output voltage of the memristor-based DC source can be tuned by changing the feedback resistance. This is achieved by individually programming each memristor placed in the feedback loop of the OpAmp, effectively building a programmable gain amplifier (PGA) whose output voltage, V_{out} , depends on the variable gain G_v :

$$|V_{out}| = \frac{R_{mem}}{R_{in}} \times V_{in} \quad (1)$$

where R_{mem} is the total feedback resistance introduced by the memristors and is given by:

$$R_{mem} = \left(\sum_i^N G_i \right)^{-1} \quad (2)$$

where i represents the index of the i -th memristor, G_i is the conductance of the i -th memristor in the feedback loop, and N the number of memristors in the feedback loop e.g., $N = 4$ in Fig. 1.

The memristors in the feedback loop can be individually programmed by using analog switches placed at room temperature; $N + 1$ switches are needed as a common top electrode is used for all memristors. The analog switch at the common top electrode allows it to connect to an arbitrary pulse measurement unit (APMU) which can send pulses to program the memristors or connect to the feedback loop of the OpAmp. Meanwhile, each memristor's bottom electrode is connected to an analog switch, enabling the grounding of the bottom electrode with an APMU for memristor programming, or shorting all bottom electrodes to create a feedback resistance with the memristors in parallel (see Fig. 1).

The cryogenic compatibility of this prototype presents two primary challenges. Firstly, finding a commercial operational amplifier capable of functioning at deep cryogenic temperatures down to 1.2 K. Secondly, validating the cryogenic compatibility of the memristors. Cryo-compatible memristors have already been demonstrated with different oxides such as HfO_x [33], [34], $HfZnO$ [35], TaO_x [36] and TiO_x [30]–[32]. In the meantime, a few commercial amplifiers have been characterized at cryogenic temperatures down to 4.2 K demonstrating cryo-compatibility. These OpAmps include the TLC271 from

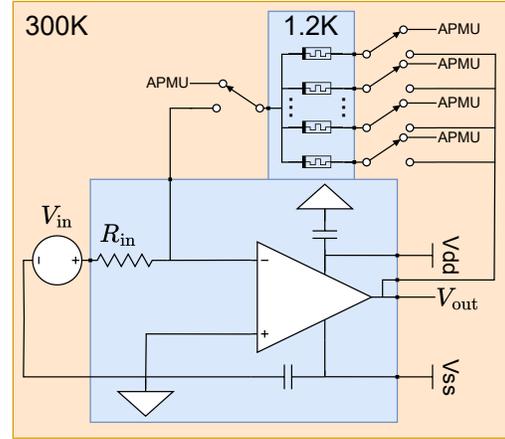


Fig. 1. **Schematic view of the memristor-based DC source prototype.** The required interconnects between cryogenic temperatures and room temperature electronics are shown as small black squares. Analog switches are used to connect the memristors to APMUs or to short them to provide resistive feedback to the OpAmp.

Texas Instruments [37], the TLV271 from onsemi, the AD8601 and AD8605 from Analog Devices [38]. Due to its low power consumption, it was decided to investigate the cryo-compatibility of AD8605 in the next section .

III. CHARACTERIZATION OF THE CRYOGENIC AMPLIFIER

The AD8605 OpAmp is tested in a typical TIA configuration, as depicted in Fig. 2a, to match the prototype presented in Fig. 1. This circuit is implemented on a 2-layer 46×39 mm FR-4 PCB (see Fig. 2b). The PCB is assembled with two resistors: $R_{in} = 1 \text{ k}\Omega$ and $R_{fb} = 2 \text{ k}\Omega$; along with two $1 \mu\text{F}$ decoupling capacitors to limit power supply noise. This PCB is placed in the 1 K-pot of an ICE Oxford DRY ICE cryostat allowing to cool down the TIA PCB to 1.2 K. Local heating can be applied to the 1 K-pot of the cryostat to increase the temperature of the PCB from 1.2 K to 300 K. A dual voltage supply of $\pm 2.7 \text{ V}$ is applied to the AD8605 OpAmp using two Stanford Research Systems DC205 high-precision DC sources. The supply voltages are maintained during the cooldown of the PCB. The supply current drawn by the AD8605 OpAmp is measured by placing a Keysight 34461A digital multimeter in series with the supply DC sources. This allows for the measurement of the power consumption of the cryogenic amplifier and the estimate of its power dissipation. The output voltage of the cryogenic amplifier is measured with a Keysight DSOX3014T oscilloscope. Four high-frequency coaxial copper lines are used to route the different signals in and out of the cryostat.

The DC behavior of the AD8605 TIA circuit is measured by sweeping the input voltage, V_{in} , from 0 V to 1.5 V. Fig. 2c shows the results at 1.2 K, 35 K and room temperature, which serves as a benchmark DC behavior. The AD8605 shows a linear TIA-like behavior at both 1.2 K and 35 K, validating the cryo-compatibility of the AD8605 OpAmp. However, the gain of the AD8605 OpAmp is observed to decrease at lower temperatures. This trend is validated by fitting the gain of the

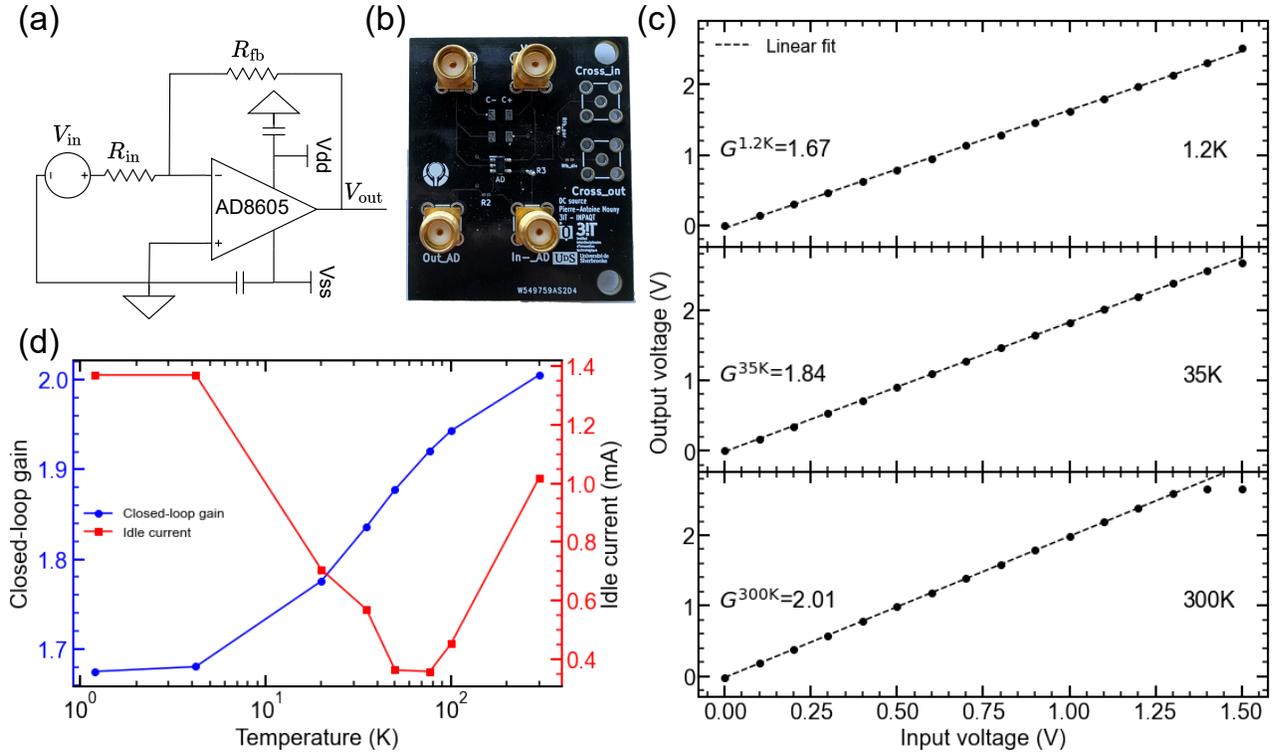


Fig. 2. **Cryogenic characterization of the AD8605 OpAmp** a. Schematic of the cryogenic TIA circuit based on the AD8605 OpAmp. R_{fb}/R_{in} define the gain of the TIA with $R_{fb} = 2 \text{ k}\Omega$ and $R_{in} = 1 \text{ k}\Omega$. b. FR-4 PCB implementation of the AD8605 TI circuits. c. DC characterization of the TIA behavior at 1.2 K, 35 K and 300 K. d. Fitted closed-loop gain (blue) and idle current (red) of the AD8605 OpAmp from 1.2 K to 300 K. The idle current is defined as the current consumption for $V_{in} = 0 \text{ V}$

TIA circuit at multiple cryogenic temperatures (see Fig. 2c). The gain of the OpAmp exhibit a logarithmic increase with temperatures between 4.2 K and 300 K. Below 4.2 K, the gain of the OpAmp plateaus roughly at 1.68. This gain decrease could partly be explained by R_{in} being a thick film resistor whose resistance increases at lower temperatures [39].

Additionally, the current consumption of the AD8605 OpAmp is measured at $V_{in} = 0 \text{ V}$ with a 50Ω load. This current is usually named idle current. As Fig. 2c depicts, the idle current of the AD8605 OpAmp is larger below 4.2 K and plateaus at 1.4 mA. Then, the idle current decreases with increasing temperature up to 77 K where it reaches a lower bound of $350 \mu\text{A}$. Finally, it increases with temperature reaching 1 mA at room temperature. The AD8605 OpAmp consumes 40% more current at 1.2 K than at room temperature for the same dual supply voltage of $\pm 2.7 \text{ V}$, leading to a power consumption of roughly 4 mW. While this power consumption is too large for scaling up the memristor-based DC source concept proposed by Mouny et al. [29], its cryo-compatibility makes it the perfect candidate for prototyping the memristor-based DC source.

IV. PROTOTYPE EXPERIMENTAL METHODS

Having established the operation of the AD8605 OpAmp at cryogenic temperatures in the preceding section, we detail the setup used to experimentally demonstrate the memristor-based DC source prototype. Fig. 3a shows a block schematic of

the experimental setup which consists of three main blocks: a control platform, the analog switches, and the DC source prototype. The control platform is a LOTUS board from Advanced MicroTesting [40] that provides 32 asynchronous APMUs and 32 General Purpose Inputs/Outputs (GPIOs). A mezzanine board with Vishay Siliconix DG4053 analog switches is fabricated to either program the memristors or connect them to the feedback loop of the TIA circuit. Finally, a 4-layer FR-4 PCB is fabricated to co-integrate the memristor chip and the TIA circuit tested previously in Section III (see Fig. 3b). The R_{in} resistor is replaced with a $3 \text{ k}\Omega$ -metallic film resistor to ensure compatibility with the memristor resistances, while R_{fb} is replaced by a memristor feedback resistance as depicted by Fig. 1.

The memristor chip is glued to a custom chip carrier. A line of two memristors sharing a common top electrode is wedge-bonded with aluminum wires to the chip carrier using a TPT HB10 semi automatic wire bonder. This number of memristor yields to the smallest form factor memristor-based DC source required for the demonstration. The memristor chip is fabricated with an etch-back process described in Ref. [41]. Similar devices have been tested at cryogenic temperatures down to 4.2 K and have demonstrated analog programmability enabled by cryogenic reforming [32]. This chip carrier is connected to the cryogenic DC source PCB using mezzanine connectors.

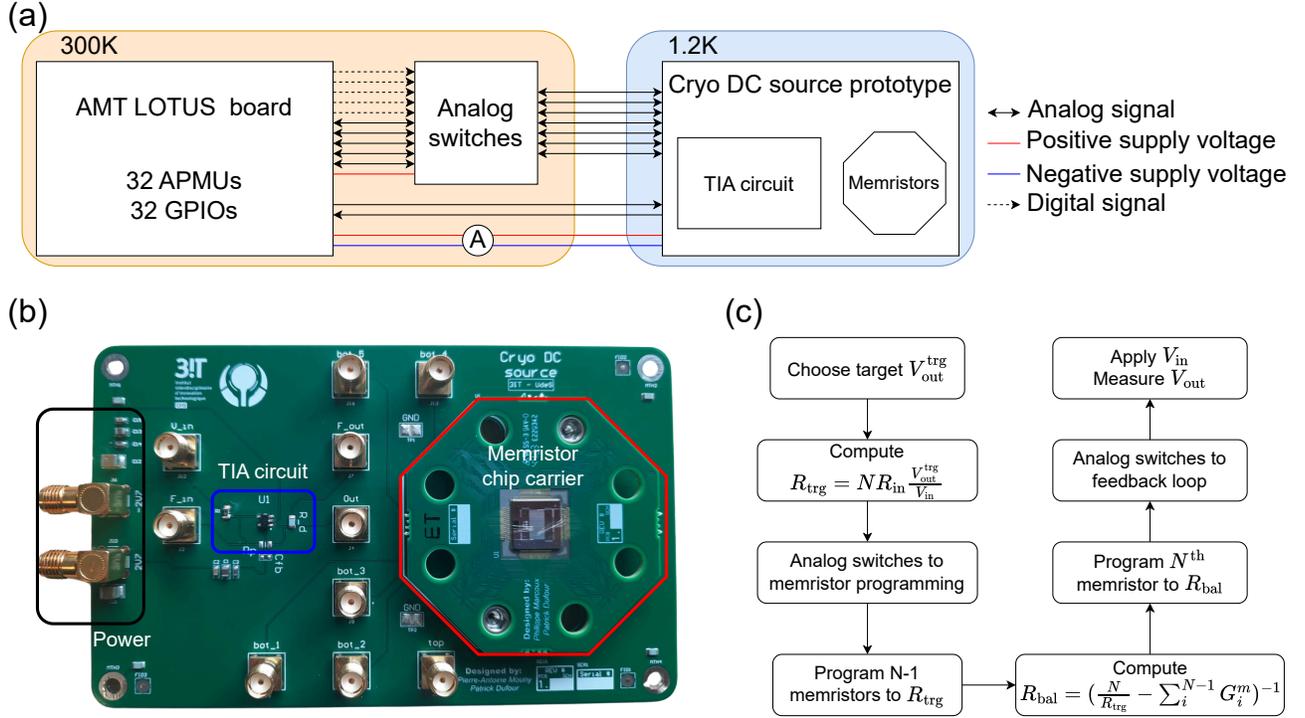


Fig. 3. **Experimental setup for the cryogenic memristor-based DC source.** **a.** Block schematic of the experimental setup used to validate the cryogenic memristor-based DC source. **b.** 4-layer FR-4 PCB implementation of the memristor-based DC source prototype. A custom chip carrier with a wire-bonded memristor chip is connected to the prototype PCB. **c.** Flowchart of the DC source prototype programming.

The output voltage of the memristor-based DC source can be tuned by following the programming flowchart depicted in Fig. 3c. Initially, a target output voltage, $V_{\text{out}}^{\text{trg}}$, is chosen which introduces a common target resistance R_{trg} for the feedback memristors to be programmed. This resistance state is given by:

$$R_{\text{trg}} = N R_{\text{in}} \frac{V_{\text{out}}^{\text{trg}}}{V_{\text{in}}} \quad (3)$$

where N is the number of memristors in the feedback loop ($N = 2$ in this case), R_{in} is the resistance placed at the input of the inverting pin of the OpAmp (see Fig. 1), and V_{in} is the input voltage of the prototype. The analog switches are set by the GPIOs of the LOTUS board to establish connections between the memristors and the APMUs allowing their programming. All memristors except one (i.e., $N - 1$ memristors) are programmed to R_{trg} using a resistance tuning read-write-verify algorithm from Alibart et al. [42]. At each step of the algorithm, a 200 ns write pulse is applied, with its polarity either increasing the resistance (negative amplitude) or decreasing the resistance (positive amplitude). A $10 \mu\text{s}/V_r$ read pulse is then applied to measure the new memristor resistance. If R_{trg} is not reached, the next write pulse amplitude is linearly increased by $s_V = 10 \text{ mV}$. Once the target resistance is reached within a tolerance of 1%, 10 read pulses are applied to the memristor to ensure the stability of the programmed state. The read pulse amplitude, V_r , is chosen to be the difference $V_{\text{out}}^{\text{trg}} - V_{\text{in}}$, as this is the voltage that will be applied to the memristors in the feedback loop of the TIA. If a typical V_r

value of 0.2 V is used, it will be impossible to accurately tune the memristor resistances to achieve a given $V_{\text{out}}^{\text{trg}}$ value due to the I-V nonlinearities of memristors [43]. The final memristor is programmed to balance the error accumulated during the programming of the other $(N - 1)$ memristors. This balancing resistance state is given by:

$$R_{\text{bal}} = \left(\frac{N}{R_{\text{trg}}} - \sum_i^{N-1} G_i^m \right)^{-1} \quad (4)$$

where $\frac{N}{R_{\text{trg}}}$ is the target feedback conductance and $\sum_i^{N-1} G_i^m$ is the sum of the conductance programmed on the $N - 1$ memristors. The same resistance tuning algorithm is used with a smaller tolerance (0.5%) to improve the final accuracy of the programmable DC source. Finally, the analog switches are set by the GPIOs to connect the memristors to the feedback loop of the TIA. To evaluate the performance of the circuit, a constant V_{in} is applied and V_{out} is measured. The V_{in} is fixed for all programmed output voltages.

For the cryogenic measurements, the cryogenic DC source PCB (see Fig. 3b) is placed in the 1 K-pot of an ICE Oxford DRY ICE cryostat. The LOTUS board and the analog switches are placed outside the cryostat in an electronic rack. The memristors and feedback loop lines are connected to 5 BeCu RF lines while the supply voltages, V_{in} and V_{out} , are connected to 4 superconducting DC lines with a cut-off frequency around 10 MHz.

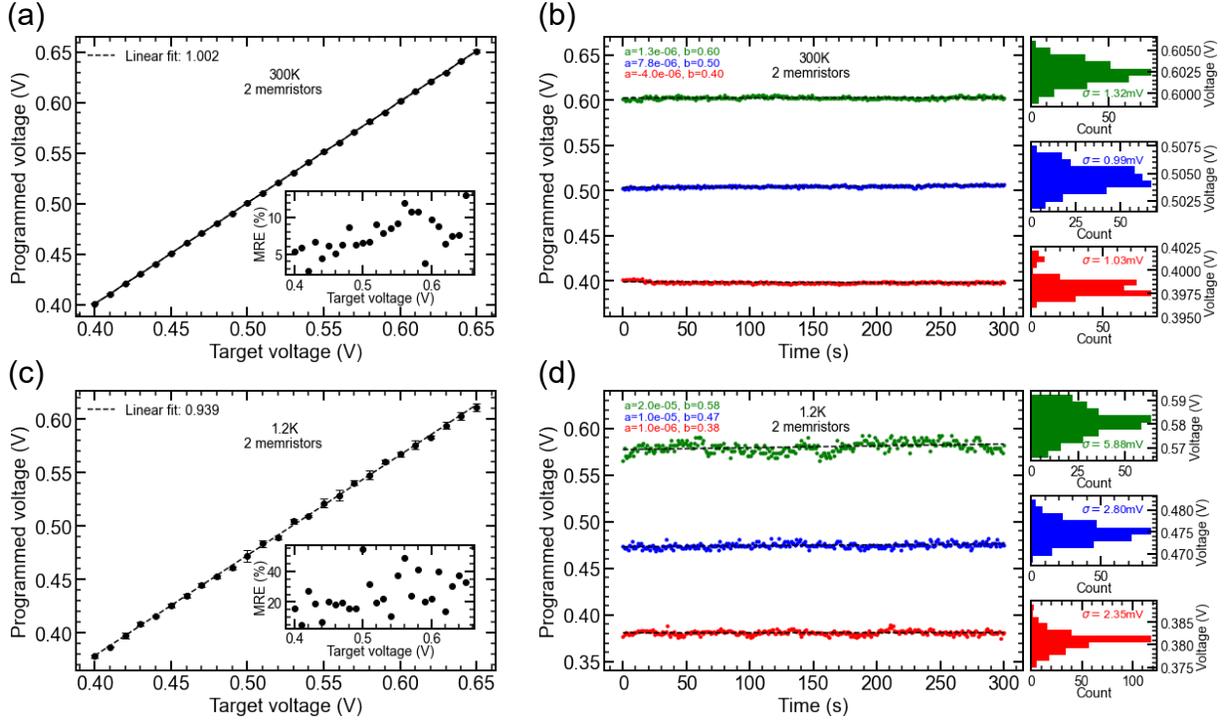


Fig. 4. **Electrical characteristics of the memristor-based DC source prototype.** **a.** A 250 mV voltage sweep between 0.4 V and 0.65 V with a resolution of 10 mV at 300 K. The experiment was performed with 2 memristors connected in parallel in the feedback loop of the TIA circuit, with $V_{in} = 0.25$ V and $V_{dd} = -V_{ss} = 2.7$ V. The voltage sweep is performed 10 times, with each point representing the mean voltage programmed while the error bars show the programming error. The mean resolution error (MRE) is shown in the inset. **b.** Stability of three intermediary programmed voltages at 300 K. Each programmed voltage is fitted by linear regression ($aV + b$) to verify the drift of the programmed voltage. The three insets depict the variability of each stable programmed voltage. **c.** Ten 250 mV voltage sweeps between 0.4 V and 0.65 V with a resolution of 10 mV at 1.2 K. The experiment was performed with 2 memristors connected in parallel in the feedback loop of the TIA circuit, with $V_{in} = 75$ mV and $V_{dd} = -V_{ss} = 3.0$ V. The inset shows the MRE for this measurement. **d.** Stability of three programmed voltages at 1.2 K. The three insets depict the variability of each stable programmed voltage.

V. EXPERIMENTAL RESULTS

In order to validate the concept of the cryogenic memristor-based DC source, the prototype has to demonstrate output voltage tunability with limited error (10% of the voltage resolution) in accordance with QD biasing requirements i.e., a 0.25–1 V output range. Hence, we performed DC sweep measurements at 300 K as a performance benchmark. The output voltage is swept between 0.4 V and 0.65 V with a resolution of 10 mV. This is achieved by running the algorithm described in Fig. 3c with $V_{in} = 0.25$ V and $N = 2$. This voltage sweep corresponds to tuning each memristor resistance between 9.6 k Ω and 15.6 k Ω . We perform 10 DC sweep measurements to assess the programming variability of the memristor-based DC source. The mean programmed voltages are reported in Fig. 4a, demonstrating the tunability of the DC source over the 0.4–0.65 V range. The DC offset (≈ 8 mV) introduced by the AD8605 operational amplifier is subtracted from the programmed voltages to mitigate systematic error. The mean programmed voltages are fitted by a linear function to verify the linearity of the output voltage. Additionally, the fitted slope ($a_f = 1.002$) allows for the quantification of the memristor feedback resistance programming accuracy. As the fitted slope is close to one, the gain of the TIA is programmed accurately. Moreover, the mean resolution error (MRE) is computed for each programmed output voltage. It

is given by:

$$\text{MRE}(V_{\text{out}}) = 100 \times \frac{\text{std}(V_{\text{out}})}{a_f \delta V} \quad (5)$$

where $\text{std}(V_{\text{out}})$ is the standard deviation of a given output voltage V_{out} over 10 sweep measurements, a_f is the fitted slope and δV is the intended voltage resolution for the sweep. The MRE for the 300 K DC sweeps is shown in the inset of Fig. 4a with an average MRE below 10% i.e., the programmed output voltage is tuned with less than a 1 mV error.

While the DC sweep measurements validate the tunability of the memristor-based DC source prototype, it is necessary to verify the stability of the programmed voltages. This can be done by measuring an arbitrary programmed output voltage over several seconds e.g., 300 s for the stability measurement reported in Fig. 4b. The time traces of the programmed voltages are fitted by a linear function ($V(t) = at + b$) to assess the stability of the output. The fitted slope factor is on the order of $5 \times 10^{-5} \text{V s}^{-1}$ which indicates a 5 μV drift every second. This drift is compatible with QD biasing as the drift timescale is very large with respect to spin qubits coherence time [9]. These stability measurements also allows for the evaluation of the voltage noise amplitude exhibited by the memristor-based DC source prototype. The three insets

of Fig. 4b show a histogram of each programmed output voltage, indicating that the voltage noise amplitude follows a Gaussian distribution with a standard deviation around 1 mV for the three tested output voltages.

The same set of measurements are performed at 1.2 K to verify the cryogenic compatibility of the memristor-based DC source prototype. Under these conditions, the TiO_x memristors used in the feedback loop need to be reformed at cryogenic temperatures to remove the metal-insulator transition hindering their analog programmability as suggested by Ref. [32]. The 10 DC sweeps measured at 1.2 K are performed with a different input voltage ($V_{\text{in}} = 75 \text{ mV}$) due to the increased resistance of the cryo-reformed TiO_x memristors at cryogenic temperatures [32]. The same DC sweep is attempted at 1.2 K i.e., a 0.4 V-0.65 V output range with a 10 mV resolution. Performing this DC sweep requires to program the two memristors between 32 k Ω and 52 k Ω . The voltage supply of the AD8605 OpAmp is increased to $\pm 3.0 \text{ V}$ to compensate for its gain loss at cryogenic temperatures (See Fig. 2c). This is not sufficient to achieve the targeted gain at each step of the sweep as the fitted slope ($a_f = 0.939$) suggests. Moreover, the inset of Fig. 4c suggests that the higher resistances of the memristors at cryogenic temperatures limits the performance of the memristor-based DC source prototype as the average MRE is approximately 2.5 times larger than the MRE at 300 K. Additionally, the current consumption of the AD8605 OpAmp was measured during the DC voltage sweeps and ranges from 1.43 mA to 1.84 mA. This yields to a power consumption of around 10 mW for the OpAmp, while the memristor resistive feedback dissipates between 6 μW and 12 μW . Assuming that most of the power consumed by the OpAmp is dissipated, the AD8605 introduces a bottleneck in power dissipation if the prototype was to be scaled up. Nonetheless, the Fig. 4c demonstrates the viability of the memristor-based DC source concept.

The stability of the programmed DC voltage was also investigated at 1.2 K (see Fig. 4d). The memristor-based DC source shows a lower voltage drift at cryogenic temperature as the slope factor a is up to an order of magnitude smaller than the one fitted at 300 K. This increases the retention of the DC source prototype to a 1 mV drift every 1000 s, which is a very large retention time when compared to the coherence time of spin qubits ($\approx 10 \text{ ms}$ [9]). This validates the edge of the memristor-based DC source concept over switched-capacitors circuits which need to be refreshed every tens of microseconds [26]. However, the programmed output voltages exhibit a larger voltage noise amplitude. This is mainly due to the larger resistance of the TiO_x memristors at 1.2 K as suggested previously [32]. The read variability introduced by memristors increases linearly with their resistance [44]. This is validated by the 300 K measurements which exhibit a voltage noise up to five times smaller with smaller memristor resistances. Electronic noise is the main concern when interfacing with quantum dots as an output voltage noise too important could lead to decoherence of the qubit [45], [46]. This output voltage

noise could be mitigated by using a low-pass filter which would not prevent the operation of the DC source as its role is to apply a DC bias to quantum dots. However, it is to be noted that such filtering would add an additional thermal load.

While the memristor-based DC source prototype shows an insufficient voltage resolution to achieve quantum dot biasing, our previous study suggests that increasing linearly the number of memristors placed in feedback loop allows to reduce the voltage resolution exponentially [29]. Namely using 8 memristors would allow to reach a voltage resolution of $\approx 100 \mu\text{V}$. This could be achieved by monolithically integrating the memristors in the feedback loop of an integrated CMOS OpAmp [47].

VI. SCALING DISCUSSIONS

The previous study performed with discrete components and a limited number of memristors serves as a proof of concept for this novel cryogenic DC source. Making this solution scalable now requires the design of a fully integrated CMOS-memristor circuit. Moving from discrete electronic components to integrated electronics will drastically reduce both the power consumption and footprint of the operational amplifier used in the memristor-based DC source. The scaling of this DC source is investigated using electronic computer-aided design and circuit simulations to estimate the DC source footprint, power consumption, and electrical characteristics. Firstly, an integrated TIA in 65 nm TSMC CMOS technology is designed (see Fig. 5a). This TIA is based on a two-stage Miller operational amplifier [48] with a memristor resistive feedback, a concept that can be extended to all emerging non-volatile memories (eNVM). For scaling purposes, the memristors should be fabricated in the back end of line of the TIA CMOS chip using CMOS-compatible fabrication processes. The initial TIA is designed to be used with a single CMOS-compatible TiO_x memristor from Ref. [32], more precisely called valence change material memory (VCM), as the resistive feedback. These VCMs demonstrate analog programmability down to 4.2 K between 10 k Ω to 100 k Ω [32]. The design parameters are reported in Table I.

TABLE I
PARAMETERS FOR THE OPAMP DESIGN USED IN FIG. 5(B). ALL TRANSISTOR LENGTH ARE SET TO 65 nm. FOR ALL SIMULATIONS IN FIG. 5(C) AND (D), R_{IN} IS EQUAL TO $R_{\text{MIN}}/4$.

Parameter	Value	Unit
I_B	1	μA
$V_{\text{in}}, V_{\text{cm}}$	100	mV
$V_{\text{dd}}, V_{\text{ss}}$	± 3	V
M_1, M_2	1.5	μm
M_3, M_4	1	μm
M_5	10	μm
M_6	380	nm
M_7	760	nm
M_8	120	nm
R_s	10	k Ω
C_s	3.5	pF
R_{in}	2.5	k Ω

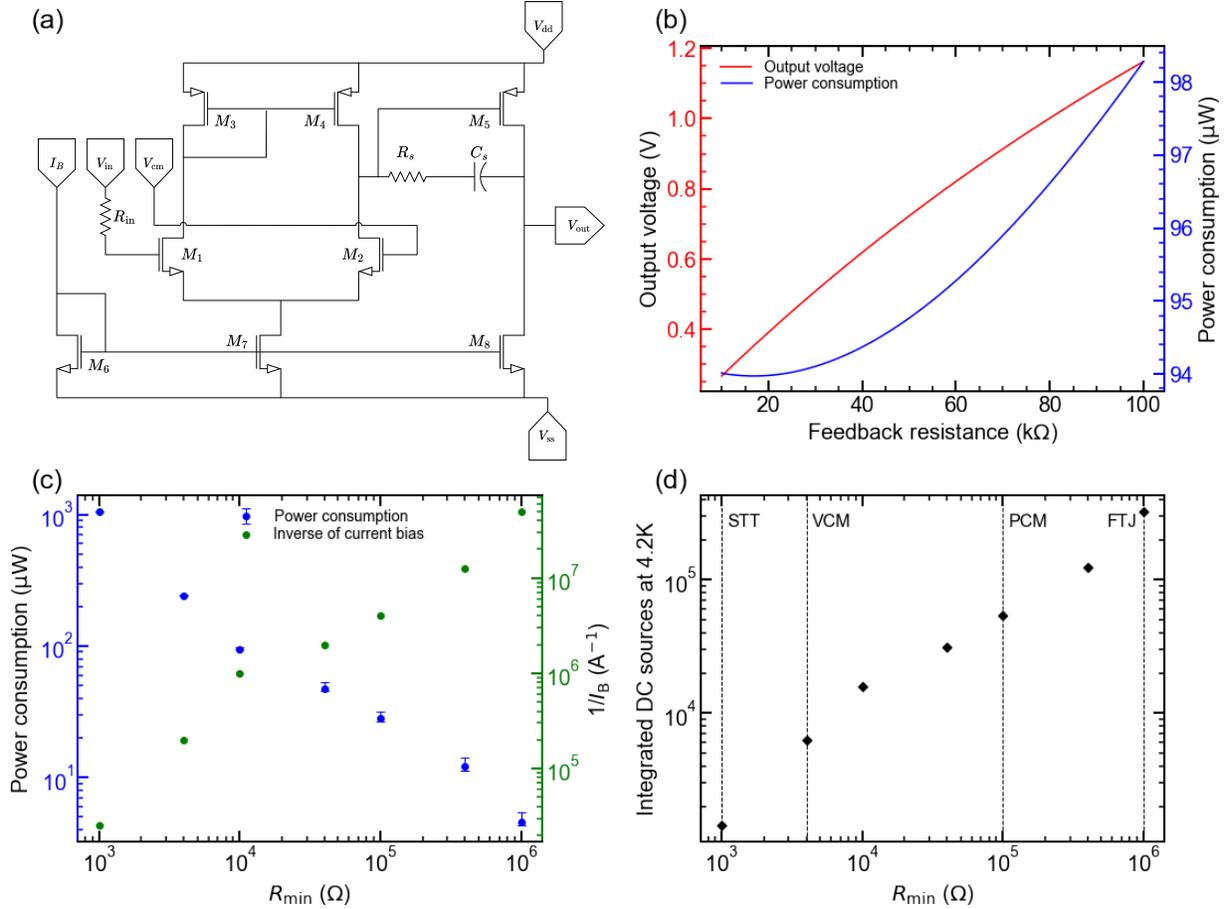


Fig. 5. **eNVM-based DC source scaling simulations.** **a.** The operational amplifier schematic based on a two-stage Miller topology. One or multiple eNVM can be placed between the V_{in} and V_{out} nodes to enable the tunability of the DC source. A single fixed resistor R_{in} is placed after the V_{in} node to allow transimpedance amplification. **b.** DC characteristics of the operational amplifier for a feedback resistance ranging from 10 kΩ to 100 kΩ. The circuit parameters used for this simulation are reported in Table I. **c** Feedback resistance scaling simulation. Larger resistances results in a decrease of the bias current I_B , leading to a power consumption decrease. **d** Maximum number of eNVM-based DC sources integrable at the 4.2 K stage of a Bluefors XLD dilution fridge i.e., a 1.5 W cooling power. The dashed black lines show the minimum resistance of different eNVM technologies.

The first stage of the TIA is composed of a stabilized differential pair biased with $2I_B$ by the M_6-M_7 current mirror. The second stage is a simple source follower biased by $\frac{1}{3}I_B$. From the room temperature DC simulations, a biasing current I_B of $1\mu\text{A}$ is needed to achieve a 1 V output range which is required for quantum dot auto-tuning. This setup yields to a sub-100 μW power consumption for a single eNVM-based DC source (See Fig. 5(b)) i.e., a 80 times smaller power consumption than the discrete prototype experimentally tested. Using the same design, the power consumption can be reduced by increasing the feedback resistance while decreasing the bias current I_B . As depicted in Fig. 5(c), this approach allows to reduce the power consumption by an additional factor of 20 by lowering I_B to 20 nA. However for $R_{min} \geq 50\text{ k}\Omega$, the width of M_5 is increased to $40\mu\text{m}$ to maintain the 0.2–1.2 V output range. This increases the footprint of the TIA by a factor of approximately 4 which could limit the integration density. This level of power consumption enables a significant scaling up of the number of eNVM-DC sources integrated at the 4.2 K stage of a dilution fridge close to ‘hot’ spin qubits [12]. Utilizing the same TiO_x VCM memory [32] would

facilitate the integration of up to 16,000 VCM-based DC sources (see Fig. 5(d)), based on a 1.5 W cooling power and considering that all consumed power needs to be dissipated. However, using alternate eNVMs, such as ferroelectric tunnel junctions (FTJ) which exhibit resistances above $1\text{ M}\Omega$ [49] and working at cryogenic temperatures [50], will allow to integrate up to 300,000 DC sources at 4.2 K. This is mainly due to the larger resistance of FTJs enabling to lower the current bias of the amplifier and thus its power consumption. Additionally, this TIA topology has been demonstrated down to 4.2 K in a smaller 28 nm fully depleted silicon on insulator (FDSOI) technological node [51]. This TIA exhibited a power consumption of $1\mu\text{W}$ for a feedback resistance in the same order of FTJ resistances. Therefore designing a custom TIA in 28 nm FDSOI node with higher eNVM resistances would allow to reduce the power consumption down to $\approx 1\mu\text{W}$ per DC source i.e., by almost 4 order of magnitude compared to the experimental prototype presented. This would enable the control of nearly to one million quantum dots, assuming two gates require biasing by quantum dots [26].

VII. CONCLUSION

In conclusion, we validate the viability of a memristor-based cryogenic programmable DC source for scalable *in-situ* quantum-dot control. The cryogenic compatibility of the commercial operational amplifier AD8605 is tested down to 1.2K. At cryogenic temperatures the AD8605 exhibit a decrease in voltage gain and an increase in current consumption. Additionally, we demonstrate that this simple control approach which includes an OpAmp and memristor devices allows to perform 0.25 V-DC sweeps with a 10 mV voltage resolution with only 2 memristors at 1.2K. The memristor-based DC source prototype shows an output voltage retention time well above the coherence time of spin qubits which is the main advantage of this concept over switched-capacitor circuits. To fulfill the baseline requirements for quantum dot biasing (i.e., a 1 mV-resolution over a 1 V-range), monolithically co-integrate memristors with advanced CMOS circuitry (OpAmp and analog switches) can be utilized to enable low power dissipation down to a few microwatts per DC source within a small footprint, closing the power consumption gap with switched-capacitors biasing circuit. By using alternate emerging non-volatile memory technologies like FTJs, scaling up this concept encompass a few hundred of thousands of eNVM-based DC source for *in situ* quantum dot biasing paving the way for large-scale quantum computing applications.

Data availability The data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

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Author contributions

Pierre-Antoine Mouny: Data curation; Investigation; Methodology; Resources; Software; Visualization; Writing – original draft; Writing – review & editing. **Raphaël Dawant:** Resources; Writing – review & editing. **Patrick Dufour:** Resources; Software; Writing – review & editing. **Matthieu Valdenaire:** Software; Writing – review & editing. **Serge Ecoffey:** Project administration; Supervision; Writing – review & editing. **Michel Pioro-Ladrière:** Funding acquisition;

Project administration; Writing – review & editing. **Yann Beilliard:** Conceptualization; Project administration; Supervision; Writing – review & editing. **Dominique Drouin:** Conceptualization; Funding acquisition; Project administration; Supervision; Writing – review & editing. **Competing interests** The authors declare no competing interests.

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