A Data-Driven Condition Monitoring Method for Capacitor in Modular Multilevel Converter (MMC)

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Abstract—The modular multilevel converter (MMC) is a topology that consists of a high number of capacitors, and degradation of capacitors can lead to converter malfunction, limiting the overall system lifetime. Condition monitoring methods can be applied to assess the health status of capacitors and realize predictive maintenance to improve reliability. Current research works for condition monitoring of capacitors in an MMC mainly monitor either capacitance or equivalent series resistance (ESR), while these two health indicators can shift at different speeds and lead to different end-of-life times. Hence, monitoring only one of these parameters may lead to unreliable health status evaluation. This paper proposes a data-driven method to estimate capacitance and ESR at the same time, in which particle swarm optimization (PSO) is leveraged to update the obtained estimations. Then, the results of the estimations are used to predict the sub-module voltage, which is based on a capacitor voltage equation. Furthermore, minimizing the mean square error between the predicted and actual measured voltage makes the estimations closer to the actual values. The effectiveness and feasibility of the proposed method are validated through simulations and experiments.

Index Terms—Condition monitoring, capacitor, data-driven, modular multilevel converter.

I. INTRODUCTION

Modular multilevel converter (MMC) attracts wide research attention in medium voltage and high voltage applications such as HVDC and STATCOM due to its high modularity, low harmonic component, high efficiency, etc [1]–[4]. Since MMC consists of a large number of components, the reliability of critical components in the MMC should be evaluated carefully. Capacitors are one of the critical components in the MMC, as they can stabilize the submodule voltage and are key elements in voltage level generation. Similar to any other component, capacitors are subjected to aging over time as they suffer from electrical and mechanical stresses during operation. The degradation can be monitored and maintenance plan can be updated accordingly. The method of scheduling the maintenance intervention based on the health status is known as predictive maintenance, which can mitigate the loss of unplanned downtime and additional maintenance costs [5]. The key to do predictive maintenance is getting a reliable and accurate health status of the critical components, where condition monitoring methods can help.

There are different approaches to monitoring the health status of capacitors in the MMC, and the main research direction is monitoring the capacitance. This is due to the fact that the voltage and current harmonics in MMC are mainly located in the low-frequency region (below a few kHz) and the capacitance dominates the equivalent circuit model in this region, so that the other components in the equivalent circuit model, namely equivalent series resistance (ESR) and equivalent series inductance (ESL), are neglected in the capacitance calculation process [6]. The capacitance can be calculated with voltage and current harmonics, and these harmonics can come from either normal operation [7]–[10] or injected harmonics [11]. The capacitance can also be calculated with a capacitance-voltage relationship based on a reference submodule, where the submodule voltage ripple is inversely proportional to the capacitance when the same switching signals are given to the submodule under test and the reference submodule [12]–[14]. It is possible that the capacitance-voltage relationship is built based on the discharging voltage curve, however, with the expenses of the exclusion of a submodule [15]. Using data-driven methods is another way to monitor the capacitance, e.g., the Kalman filter [16] and recursive least square [6], which needs a more complicated structure than model-based methods.

Besides the capacitance, ESR in the equivalent circuit model can also be used to monitor the health status since ESR can deteriorate faster than the capacitance and reaches the end-of-life criteria much earlier than the capacitance, as reported in [17]–[20]. In these cases, if the condition monitoring method only monitors capacitance, the converter might operate with a degraded capacitor that has a high ESR, and the end-of-life warning is not triggered until the capacitance reaches the end-of-life criteria which makes the estimated health status unreliable. Considering the importance of monitoring ESR in reflecting the capacitor degradation, recently published research has started to monitor the ESR for capacitors in an MMC, e.g., by using the wavelet decomposition to analyze the turn-on transient voltage step which requires extra components

to measure the fast and small voltage step [21] and the harmonic-based method [22].

There are certain limitations in the existing methods: 1) only monitoring a single health indicator, e.g., [7]–[14]. Considering the capacitance and ESR can shift at different speeds, the end-of-life time indicated by them can be different. For instance, if ESR degrades faster than the capacitance, the end-of-life time related to ESR will be shorter than the one related to capacitance. Between these two end-of-life times, the end-of-life warning is not triggered if only monitoring the capacitance even though the actual ESR already exceeds the end-of-life criteria. 2) the normal operation of the converter is affected during the condition monitoring due to changes in the control behaviors, e.g., [12]–[14].

To solve these problems, this paper applies a data-driven condition monitoring method to monitor capacitance and ESR together, so the health status can be derived no matter which health indicator (capacitance or ESR) degrades faster. The reason for using capacitance and ESR as health indicators is that these two health indicators cover the main failure mechanism, i.e., electrolyte evaporation of the aluminum electrolytic capacitor which is suitable for MMC applications [23]. Adding more health indicators makes the condition monitoring method more complicated without covering more failure mechanisms. For instance, the weight of the capacitor decreases as the electrolyte evaporates. However, measuring the weight requires disassembling the capacitor from the print circuit board, and the weight is less sensitive than the capacitance and ESR [24], [25].

Specifically, the proposed method uses particle swarm optimization (PSO) to update the position of particles, where the positions are estimated capacitance and ESR. Then the estimations are used to predict the submodule voltage in a sampling window based on a capacitor voltage equation. The mean square error between the predicted and measured submodule voltage is used as the objective function. The update process reduces the voltage prediction errors, and in the meantime, the estimations of health indicators are closer to the actual values.

Compared with the existing methods, the proposed method has the advantages of:

- Monitoring both capacitance and ESR so the condition monitoring result is more reliable compared with methods based on one of the health indicators.
- The method runs offline so the normal operation of the converter is not affected, and it requires no extra components.

The system description is given in Section II; the proposed method is introduced in Section III; and validations are provided in Sections IV-V.

II. SYSTEM DESCRIPTION

This section introduces the MMC topology and operation, as well as the failure mechanism and health indicators of capacitors.
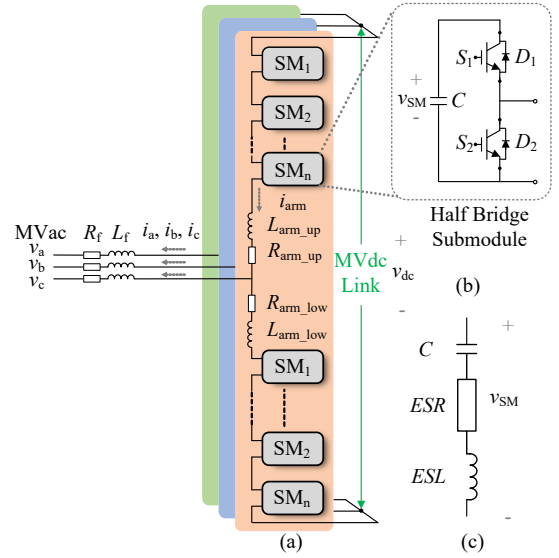

Fig. 1. A modular multilevel converter, (a) Converter topology, (b) half-bridge submodule, and (c) model of the submodule capacitor with parasitic parameters.

A. Modular Multilevel Converter (MMC)

Three-phase MMC with one phase in detail is depicted in Fig. 1(a). As demonstrated, three phases are connected with a medium voltage ac grid (v_a, v_b, and v_c) with a filter inductor L_f and a filter resistor R_f. Each phase of MMC is composed of two arms, known as the upper and lower arms. A series of connections of submodules with an arm inductor L_{arm} and equivalent arm resistor R_{arm} forms an arm. The topology of the half-bridge submodule is shown in Fig. 1(a), which consists of a capacitor and two IGBTs with their antiparallel diode, namely C, S_1, S_2, D_1, and D_2, respectively.

The MMC can be used as an inverter or an active front-end rectifier, where the outer control loop is responsible for it. In a typical MMC controller, the generated current references are considered as inputs of the inner control loop. Then, the reference of the arm voltages is produced and used in the modulation step. Apart from the mentioned controllers, MMC exploits some other controllers to improve the performance of the submodules, such as circulating current control, energy balancing control, etc. [26], [27].

B. Failure Mechanism of Capacitors

The capacitor being analyzed in this section is limited to the aluminum electrolytic capacitor (AEC), which is suitable for MMC applications because of its high energy density and relatively low cost [23].

The capacitor can experience electrical stress (e.g., voltage and current ripple) and thermal stress in the operation stage. For AECs, these stresses can lead to electrolyte evaporation, oxide film degradation, and anode foil degradations [19].

The degradation mechanisms can be monitored with electrical or non-electrical health indicators. The electrical indicators, e.g., capacitance and ESR, can be measured online and they
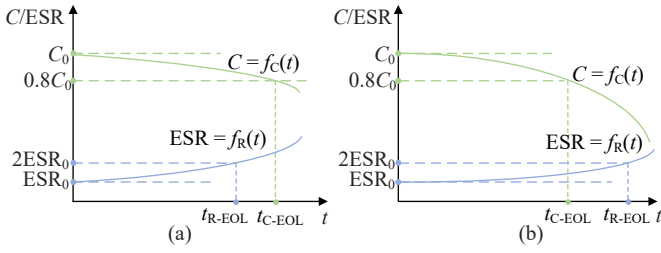
Fig. 2. Health indicators of capacitors changing gradually with operation time. When the capacitance reduces to 0.8 of the initial value C_0 or the ESR increases to two times the original ESR_0, the capacitor reaches the end-of-life time t_{C-EOL} or t_{R-EOL}, respectively. (a) ESR reaches the end-of-life criteria earlier than the capacitance, and (b) Capacitance reaches the end-of-life criteria earlier than the ESR.

have a clear relation with the end-of-life criteria. While the non-electrical indicators, e.g., weight and pressure, are difficult to measure online and require a conversion stage to estimate the remaining useful lifetime. Therefore, using electrical indicators to estimate the health status is main research direction in capacitor condition monitoring.

For the AEC, the capacitor reach the end-of-life time if one of these criteria is satisfied [23]:

- Capacitance reduces to 80% of the initial value;
- Equivalent series resistance increases to 200% of the initial value.

The equivalent circuit of the capacitor is given in Fig. 1(c), consisting of a main capacitance C, an equivalent series resistance ESR, and an equivalent series inductance ESL. The capacitance and ESR affect the impedance when the frequency is below a few MHz so the ESL is negligible. The degradation process and the shifting of these two parameters are shown in Fig. 2(a)-(b), where C reduces gradually from the initial value C_0 to 80% of C_0 at time t_{C-EOL}, and the ESR increases from the initial value ESR_0 to 200% ESR_0 at t_{R-EOL}.

The figure shows also that these two indicators can vary at different speeds so they reach the end-of-life criteria at different times, i.e., $t_{C-EOL} \neq t_{R-EOL}$.

Fig. 2(a) shows the ESR degrades faster than C so $t_{R-EOL} < t_{C-EOL}$ and Fig. 2(b) shows the opposite trend so that $t_{R-EOL} > t_{C-EOL}$. The worst case is that the condition monitoring method only monitors the health indicators that degrade slower, e.g., only monitor C in Fig. 2(a) so the end-of-life condition can not be detected at time t_{R-EOL}. From t_{R-EOL} to t_{C-EOL}, ESR exceeds the end-of-life criteria, which can generate higher losses and lead to capacitor failure, but the end-of-life time warning can only be triggered at t_{C-EOL}.

III. CONDITION MONITORING METHOD

To overcome the limitations in the previous capacitor condition monitoring methods, this paper proposes a method to estimate the two health indicators (being capacitance and ESR) together, while not affecting the converter operation.

The system diagram of the proposed method is illustrated in Fig. 3(a). The proposed method starts with taking input signals

and initializing capacitance and ESR which are randomly distributed in the solution space. Then the capacitance and ESR are updated with particle swarm optimization, and the updated estimations are used to predict the submodule voltage within a sampling window based on the capacitor voltage equation. The mean square error between the predicted and measured voltage is calculated and compared with an error limit to determine if the update should continue. The condition monitoring method is repeated multiple times (R_m) and the median values of these estimations are taken as the final estimations to avoid using an outlier as the final estimations. The key modules in the flowchart are introduced in the following sections.

A. Input Signal

Three signals related to one submodule being monitored are measured, including the submodule voltage $v_{SM}(t_k)$, the switching state of the submodule $v_{sw}(t_k)$, and the arm current $i_{arm}(t_k)$.

An example waveform is shown in Fig. 3(b). These three signals are time series in a sampling window, $t_k = t_1, t_2, ..., t_N$. The sampling window is selected as half of the fundamental cycle within which there are some switching transients because it is important for ESR estimation [21], while the window is shorter than a fundamental cycle to mitigate the error in the voltage prediction process. The sampling frequency is $100\,\mathrm{kHz}$, which is much higher than the switching frequency of an MMC (usually lower than several kHz [28]) to ensure the prediction accuracy.

B. Update C and ESR with Particle Swarm Optimization

Particle swarm optimization (PSO) is a classical metaheuristic search method. It searches the solution space with a group of particles and the positions of the particles are updated gradually with shared information to find the optimal solution.

In the proposed method, each particle has a 2-dimensional position: estimated capacitance and ESR. These two values are assigned randomly within the solution space during the initialization stage, marked as green circles in Fig. 3(c). Each particle also has a randomly given initial velocity. The position of each particle leads to an individual voltage error. In each iteration, particles update their velocities and positions [29]:

$$v_j = \omega_j v_{j-1} + c_1 r_{1j}(x_p - x_{j-1}) + c_2 r_{2j}(x_g - x_{j-1})$$
$$x_j = x_{j-1} + v_j \tag{1}$$

where v_j and v_{j-1} are velocities, x_j and x_{j-1} are positions of the jth and $(j-1)^{th}$ iteration, respectively; x_p and x_g are individual and global optimal positions; ω_j, c_1, and c_2 are inertia weight, cognitive weight and social weight, respectively; r_{1j} and r_{2j} are two random numbers between 0 and 1, varying in each iteration. The inertia weight ω_j decreases gradually so that as the iteration increases, the velocity reduces and the searching step becomes more refined [29]. The reducing velocity can be seen on the trajectory, which moves in a wider range at the beginning and becomes more stable at the end. Three simplified trajectories are plotted in Fig. 3(c) as green dashed lines.
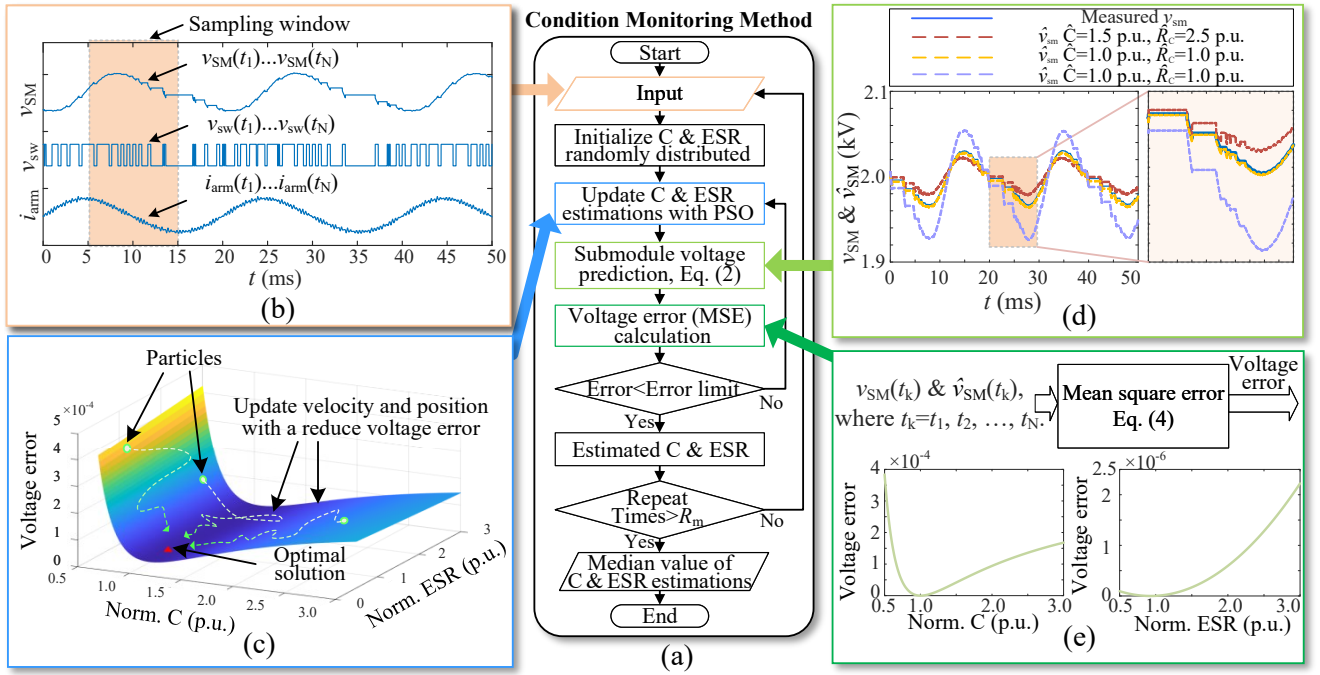
Fig. 3. A system diagram of the proposed condition monitoring method: (a) a flowchart of the condition monitoring method; (b) a sampling window of three input signals: the submodule voltage $v_{SM}(t_k)$, the switching state $v_{sw}(t_k)$, and the arm current $i_{arm}(t_k)$, where time $t_k = t_1, t_2, ..., t_N$ consists of N points; (c) the particle swarm optimization (PSO) method updates the positions of each particle to have a low voltage error; (d) the voltage prediction module predicts the submodule voltage $\hat{v}_{SM}(t_k)$ in the sampling window, where the prediction with 1 p.u. estimations is closer to the measured voltage; (e) the mean square error between predicted and measured voltage error is calculated, and it is minimized when both C and ESR are 1 p.u.

Eq. 1 shows that the positions are updated according to the global and individual optimal solution, so the voltage errors of all particles reduce gradually and the positions of particles move to the optimal solution gradually. In other words, the update process uses particles to approach the actual values.

C. Voltage Prediction and Error Calculation

The voltage prediction block takes the measured signals (i.e., $i_{arm}(t_k)$ and $v_{sw}(t_k)$) as well as the estimated parameters (i.e., $\hat{C}$ and $\hat{R}_C$) to predict a series of submodule voltage $\hat{v}_{SM}(t_k)$, where $t_k = t_1, t_2, ..., t_N$ covering the entire sampling window. At the first time step t_1, $\hat{v}_{SM}(t_1) = v_{SM}(t_1)$. The prediction starts from the second time step t_2 to the last time step t_N in the sampling window, and the prediction is based on a capacitor voltage equation:

$$\hat{v}_{SM}(t_k) = \hat{v}_{SM}(t_{k-1}) + \frac{i_c(t_k)T_s}{\hat{C}} + \hat{R}_C[i_c(t_k) - i_c(t_{k-1})] \tag{2}$$

where T_s is the sampling time; $i_c(t_k)$ is the capacitor current and it is the product of the arm current and the switching state:

$$i_c(t_k) = i_{arm}(t_k)v_{sw}(t_k) \tag{3}$$

where the switching state $v_{sw}(t_k)$ is one when the upper switch of the submodule is turned on and the capacitor is in the charging/discharging state; while $v_{sw}(t_k)$ is zero when the

lower switch in the submodule is turned on and the capacitor is bypassed.

The prediction is evaluated with the mean square error between the predicted submodule voltage $\hat{v}_{SM}(t_k)$ and the measured voltage $v_{SM}(t_k)$.

$$V_{err} = \frac{1}{V_m^2 N} \sum_{t_k=t_1}^{t_N} (v_{SM}(t_k) - \hat{v}_{SM}(t)_k)^2 \tag{4}$$

where V_m is the maximum measured submodule voltage within the sampling window and N is the number of time steps in the sampling window.

The submodule voltage error is compared with an error limit to determine if the capacitance and ESR estimations should be updated. A large error indicates that the estimations deviate significantly from the actual value while a small error reveals that the estimations are close to the actual values. Fig.3(d) shows the voltage prediction waveforms. When the estimated capacitance and ESR are different from 1 p.u., the prediction waveforms in dashed lines significantly deviate from the measured voltage (a solid blue line). The voltage error against the normalized capacitance and ESR when their counterparts are 1 p.u. are given in Fig. 3(e), which shows that the voltage error is minimized when both estimations achieve 1 p.u.

IV. SIMULATION STUDY

This section validates the design, which is the selection of swarm size and error limit for the data-driven condition

TABLE I
SIMULATION AND EXPERIMENTAL SETUP PARAMETERS.

Parameter	Var.	Simulation	Experimental
Input power	P_{in}	3 MW	N/A
DC voltage	V_{DC}	40 kV	200 V
AC voltage	V_{AC}	16.5 kV	N/A
AC frequency	f_g	50 Hz	50 Hz
SM switching frequency	f_{sw}	3 kHz	1 kHz
Full bridge switching frequency	f_{cg}	N/A	10 kHz
Filter inductance	L_f	40 mH	5.4 mH
Arm inductance	L_{arm}	10 mH	N/A
Filter resistance	R_f	100 mΩ	1 Ω
Arm resistance	R_{arm}	100 mΩ	N/A
Number of SM per arm	-	20	1
SM capacitance	C	2.2 mF	2.26 mF
SM capacitance ESR	ESR	40 mΩ	44.12 mΩ
Sampling window	-	10 ms	10 ms
Sampling frequency	f_{sa}	100 kHz	100 kHz
Voltage loop bandwidth	f_v	N/A	20 Hz
Current loop bandwidth	f_i	800 Hz	800 Hz
Repeat times	R_m	15	15
Swarm size	-	10	10
Error limit	-	10^{-6}	10^{-6}
Maximum iteration	-	100	100
Cognitive weight	c_1	1.49	1.49
Social weight	c_2	1.49	1.49
Boundary of C estimation	-	$[1.1, 6.6]$mF	$[1.1, 6.6]$mF
Boundary of ESR estimation	-	$[20, 120]$mΩ	$[20, 120]$mΩ

Fig. 4. MMC simulation waveforms of (a)three-phase grid voltage, (b) three-phase arm current, (c) arm current in phase A, (d) submodule voltage of the upper and lower arm in the phase a.

monitoring method, and the result which includes voltage predictions and health indicator estimations.

A. Simulation Setup

The condition monitoring method is validated with a three-phase MMC simulation model built in PLECS. The circuit model and parameters are listed in Table I and the MMC converter is operating in the rectifier mode at full load, i.e., $P_{in} = 3$ MW. The key waveforms are illustrated in Fig. 4. The current is regulated by a current controller where it can be seen that the grid current (i_a, i_b, and i_c) is in phase with the phase voltage (v_a, v_b, and v_c). The upper and lower arm currents (i_{armu} and i_{arml}) are balanced by a circulating current controller. The submodule voltage is controlled with a sorting method to balance the submodule voltages of 20 submodules in one arm ($v_{SMu1-20}$ and $v_{SMl1-20}$).

After running the simulation model, the signals of the submodule voltages, arm current, and switching signals are recorded for condition monitoring purposes.

B. Parameter Design of Data-driven Condition Monitoring

To tailor the optimization method for condition monitoring, the effect of two parameters is studied: the number of swarms (also named the swarm size), and the error limit.

The swarm size is usually between 20 and 30 [29] therefore 30 is the maximum swarm size to be studied. The test conditions are listed in Table I, and the capacitor has capacitance and ESR at their initial values, 1 p.u. The condition monitoring method repeats for a hundred times to visualize the distribution of estimations, as shown in Fig. 5.

The scatter plot and the boxplot illustrate the distribution of estimations. With an increasing swarm size, the estimations (blue dots) concentrate gradually. The box plots also illustrate the concentration of estimations; the height of the
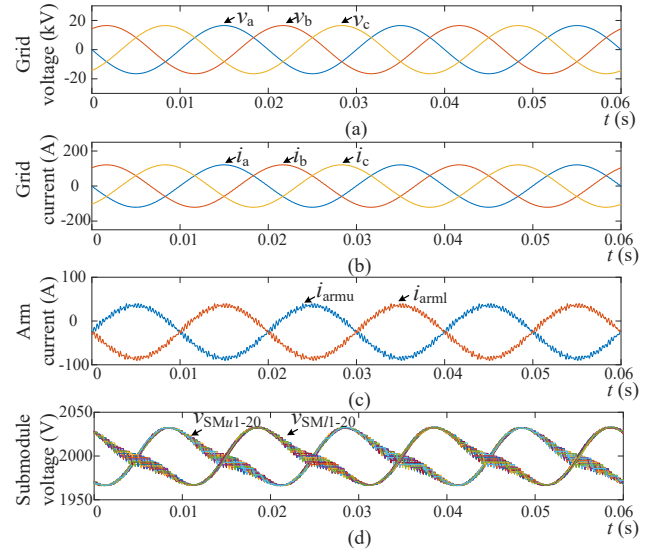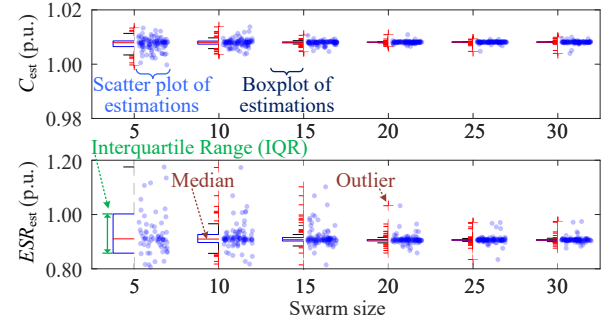

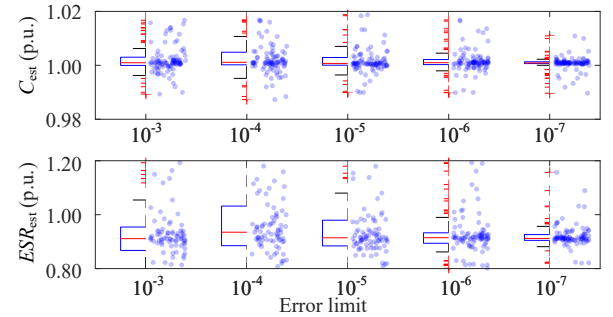Fig. 5. The effect of the swarm size on estimation results distribution.

Fig. 6. The effect of the error limit on estimation results distribution.

box (named the interquartile range or IQR) covers most of the estimations and reduces gradually with increased swarm sizes. For instance, if the swarm size is 5, the interquartile ranges of capacitance and ESR estimations are 0.21% and 14.47% of 1 p.u., respectively; while if the swarm size is 10, these values are 0.11% and 2.95%, respectively. Considering the acceptable error ranges for C and ESR are $\pm1\%$ and $\pm10\%$, respectively [22], the IQR of ESR when the swarm

size is 5 is $14.47\,\%$ which is higher than the acceptable error range $\pm 10\,\%$. Therefore, it is better to have a larger swarm size, and the swarm size is selected as ten, which gives stable estimations in the acceptable error range.

The second parameter that needs to be considered is the error limit. The error limit is usually in the range of 10^{-3} and 10^{-7}, and its effect on estimations and iterations are shown in Fig. 6. When the error limit reaches 10^{-6}, both capacitance and ESR estimations concentrate around the median value, with interquartile ranges of $0.19\,\%$ and $3.86\,\%$, respectively. Therefore, the error limit is selected as 10^{-6}.

C. Voltage Prediction

The voltage prediction function is validated in the full load condition with two capacitors: a healthy capacitor ($C = \text{ESR} = 1$ p.u.) and a fully degraded capacitor ($C = 0.8$ p.u. and ESR = 2.0 p.u.).

The sensed voltage is compared with the predicted voltage in Fig. 7(a). The voltage prediction in dashed lines can follow the voltage measurement in solid lines with an instantaneous voltage error below $2\,\text{V}$, which is $0.1\,\%$ of the $2\,\text{kV}$ average submodule voltage, as seen in Fig. 7(b). In the zoomed-in waveform on the right side, voltage steps caused by current steps during the switching transient can be seen. The magnitude of the voltage step is proportional to the ESR (Eq. (2)) so the degraded capacitor has a higher voltage step because of the higher ESR.

Considering the voltage error is below $2\,\text{V}$ or $0.1\,\%$ of the $2\,\text{kV}$, the estimation error is acceptable and should only affect the capacitance and ESR estimations in a limited range.

D. C and ESR Estimation

This section validates the function of capacitance and ESR estimation with different health statuses. The test condition is that C and ESR vary linearly between the healthy condition and the end-of-life criteria:

- C: 1, 0.99, ..., 0.8 p.u.
- ESR: 1, 1.05, ..., 2 p.u.

The solution space is half and three times the nominal value (i.e., $\hat{C} \in [0.5,3]$ p.u. and $\hat{R}_C \in [0.5,3]$ p.u.) to cover both the end-of-life criteria and a $\pm 20\,\%$ tolerance.

The condition monitoring method repeats 15 times for 20 submodules in the upper arm of phase A, and all normalized estimations are illustrated with boxplots in Figs. 7(c) and (d). The acceptable estimation ranges, $1 \pm 1\,\%$ and $1 \pm 10\,\%$ for capacitances and ESRs, respectively, are colored with a white background, while the other ranges are marked with a light red background. The median values of estimations are red lines, and a green line at 1 p.u. is added as a reference. The median values for the 20 monitored capacitors are in the acceptable range. In total, the average estimation errors of capacitance and ESR are $0.18\,\%$ and $5.47\,\%$.

The boxplot can also show the distribution of all estimations; the blue box represents the $\pm 25\,\%$ range around the median value. For the capacitance and the ESR estimations, most of the blue boxes are in the ranges of $\pm 1\,\%$ and $\pm 10\,\%$,
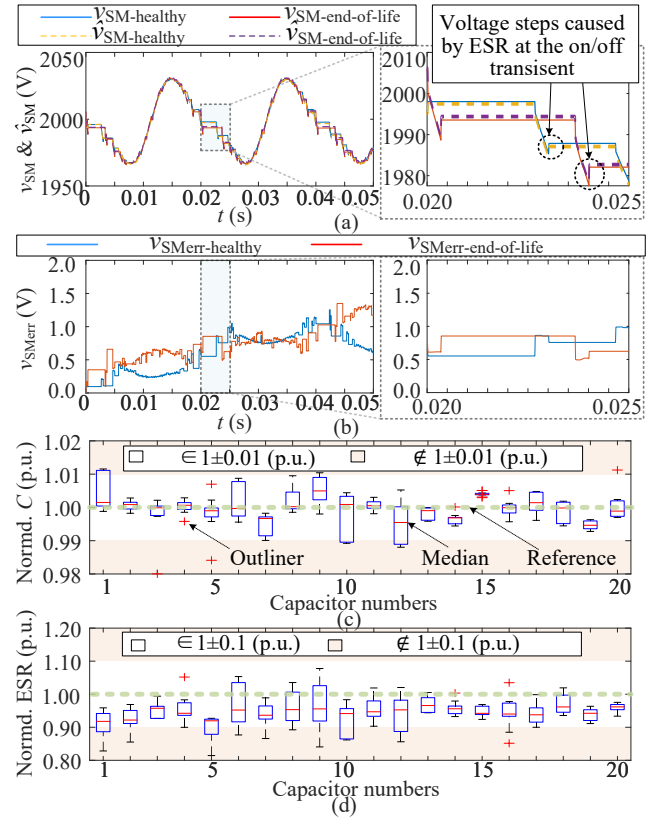

Fig. 7. Simulation results: (a) waveforms of the sensed submodule voltage v_{SM} (solid lines) and predicted submodule voltage $\hat{v}_{SM}$ with different capacitances and ESRs (dashed lines); (b) the instantaneous error between v_{SM} and $\hat{v}_{SM}$; (c) and (d) are boxplots of the estimated capacitances and ESRs.

which shows that the condition monitoring method can have acceptable estimations during most of the iterations.

V. EXPERIMENTAL RESULT

A. Test Setup

Experiments are carried out with a mission profile emulator (MPE). The MPE is a simplified reliability test setup; it emulates a mission profile for the submodule under test similar to the full MMC operation. It can reduce the required testing time and cost for building and testing an entire MMC converter because an MMC usually has a large number of components and complicated control schemes.

The mission profile emulator MPE parameters are listed in the experimental column of Table I and the control diagram is illustrated in Fig. 8(a). The MPE includes a DC voltage supply, a full-bridge current generator, a filter inductor L_f, a filter resistor R_f, and a submodule for testing (also named the device under test or DUT). There are two control loops in the control diagram, a current control loop and a voltage control loop. The current controller gets the reference current from the simulation and regulates the filter current i_{arm} by controlling the full-bridge current generator; while the voltage controller maintains the DC component in the submodule
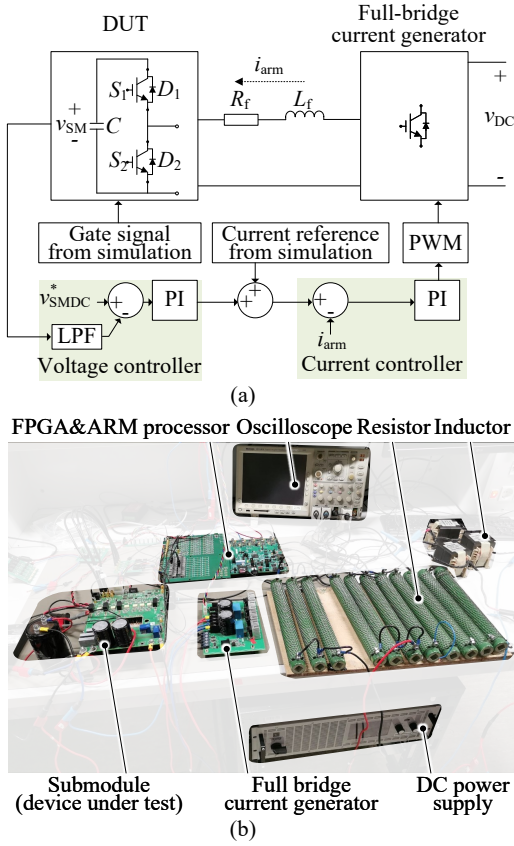
Fig. 8. Mission profile emulator test setup: (a) Topology and control diagram of the mission profile emulator used to validate the method. (b) Test setup.

TABLE II
EXPERIMENTAL TEST CONDITIONS AND ESTIMATION ERRORS OF CAPACITANCE AND ESR.

Test scenario	1	2	3	4	5	6
V_{SMDC}^* (V)	50 V			30 V		
I_{AC}^* (A)	9	6	3	9	6	3
C_{err} (%)	-0.65	-0.63	1.84	-0.43	1.02	2.39
ESR_{err} (%)	2.28	-4.46	-4.45	5.01	8.15	5.85

voltage v_{SM} by adding an offset v_{SMDC}^* to the voltage reference. Therefore, the filter current i_{arm} includes a DC component and an AC component.

The MPE test setup is illustrated in Fig. 8(b). The submodule voltage v_{SM} and the filter current i_f are sensed with a voltage divider and a current sensor LEM CKSR 15NP, respectively. These signals are sent to the controller implemented on an FPGA and an ARM processor on a ZedBoard for control purposes. They are also sent to the oscilloscope and saved for condition monitoring validation. The DUT is connected to a group of three aluminum electrolytic capacitors. The overall capacitance is $2.26\,\mathrm{mF}$ and the ESR is $44.12\,\mathrm{m\Omega}$ which are measured with an impedance analyzer Keysight E4990A.

B. Experimental Result and Discussion

The experiments are designed to validate that the proposed method can provide accurate estimations under different load
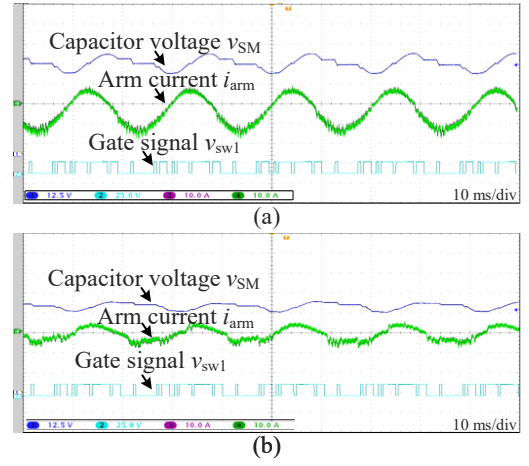

Fig. 9. Experimental waveforms: (a) test scenario 1 and (b) test scenario 3.
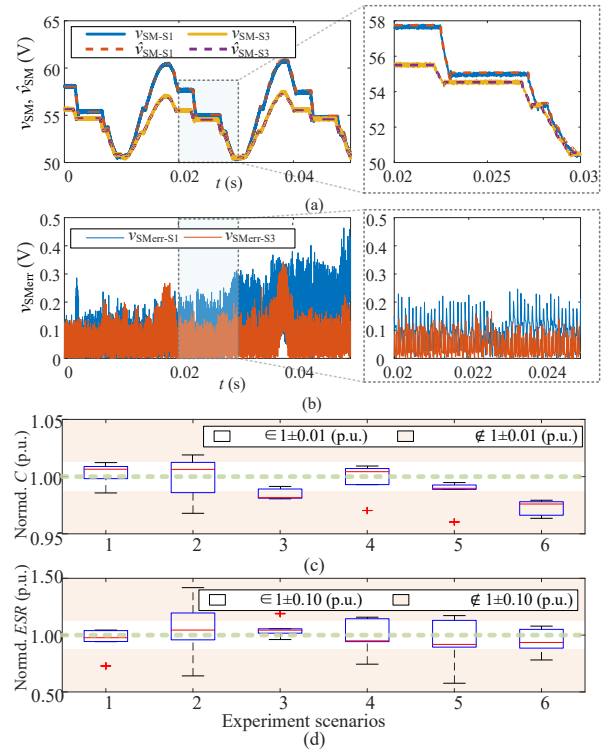

Fig. 10. Comparison between the measured submodule voltage and the predicted submodule voltage. (a) The measured and estimated submodule voltage waveforms for scenario 1 and scenario 3 in $0.05\,\mathrm{s}$; (b) The voltage error between the measurement and estimation; (c) and (d) are boxplots of capacitance and ESR estimations in six scenarios. respectively.

conditions. The testing scenarios are listed in Table II, showing the DC component of the submodule voltage varies from $50\,\mathrm{V}$ to $30\,\mathrm{V}$, and the magnitude of the AC reference current varies between $9\,\mathrm{A}$, $6\,\mathrm{A}$, and $3\,\mathrm{A}$. The operating waveforms for the first and the third test scenarios, including the submodule voltage v_{SM}, the filter current i_f, and the switching signal of the upper switch v_{sw1} are shown in Fig. 9.

To verify the function of the voltage prediction block, the

predicted submodule voltage $\hat{v}_{SM}$ is compared with the voltage measurement v_{SM}, as shown in Fig. 10. The voltage error v_{SMerr} is the instantaneous difference between the prediction $\hat{v}_{SM}$ and the measurement v_{SM}. As seen in Fig. 10(c), v_{SMerr} increases as the prediction time increases, but the error is lower than $0.5\,\mathrm{V}$ within a $0.05\,\mathrm{s}$ period.

The normalized capacitance C and ESR estimations are given in Figs. 9(c) and (d), wherein the green dashed line is the reference value; the red line is the median estimation; the blue box represents the $\pm 25\,\%$ estimations; the whisker above and under the box means outliers of estimations; the red areas are the range above $\pm 1\,\%$ and $\pm 10\,\%$ for the C and ESR, respectively. Except for test scenario 3 and test scenario 6, the median values of estimated capacitance and ESR are around $\pm 1\,\%$ and $\pm 10\,\%$, respectively. The higher error of C for test scenarios 3 and 6 can come from the small voltage ripple as shown in Fig. 9 (b). These estimation errors are listed in Table II. Compared with simulation results in Figs. 7(c) and (d), the experimental results in Fig. 9 have a wider blue box, meaning that the results have higher oscillations.

VI. CONCLUSION

Based on the fact that health indicators can change at different speeds and lead to different end-of-life times, this paper proposes a condition monitoring method that can monitor both capacitance and ESR, which makes the condition monitoring results more reliable compared with other methods that monitor only one of them. The method combines the particle swarm optimization and the capacitor voltage prediction functions. The design of key parameters (swarm size and error limit) is studied to guarantee that the estimation errors of capacitance and ESR are in the expected ranges. The effectiveness of the method is validated in the simulations and experimental stages. Except for light-load cases, the estimation errors of the capacitance and ESRs are around $1\,\%$ and $10\,\%$, respectively.

REFERENCES

[1] J. A. Ansari, C. Liu, and S. A. Khan, "MMC Based MTDC Grids: A Detailed Review on Issues and Challenges for Operation, Control and Protection Schemes," *IEEE Access*, vol. 8, pp. 168154–168165, 2020.

[2] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, 2014.

[3] A. A. Z. Diab, T. Ebraheem, R. Aljendy, H. M. Sultan, and Z. M. Ali, "Optimal Design and Control of MMC STATCOM for Improving Power Quality Indicators," *Applied Sciences*, vol. 10, p. 2490, Apr. 2020.

[4] M. Hassanifar, V. M. Hrishikesan, J.-H. Jung, S. Bazyar, H. Beiranvand, T. Pereira, M. Langwasser, and M. Liserre, "Modular multilevel converters enabling multibus dc distribution," in *2023 IEEE 17th Int. Conf. Compat. Power Electron. Power Eng.*, pp. 1–7, June 2023.

[5] K. M. Sundaram, S. Padmanaban, J. B. Holm-Nielsen, and P. Pandiyan, *Photovoltaic Systems: Artificial Intelligence-Based Fault Diagnosis and Predictive Maintenance*. CRC Press, 2022.

[6] I. Polanco and D. Dujic, "Condition Health Monitoring of Modular Multilevel Converter Submodule Capacitors," *IEEE Trans. Power Electron.*, vol. 37, pp. 3544–3554, Mar. 2022.

[7] C. Liu, F. Deng, Q. Yu, Y. Wang, F. Blaabjerg, and X. Cai, "Submodule Capacitance Monitoring Strategy for Phase-Shifted Carrier Pulsewidth-Modulation-Based Modular Multilevel Converters," *IEEE Trans. Ind. Electron.*, vol. 68, pp. 8753–8767, Sept. 2021.

[8] D. Ronanki and S. S. Williamson, "Failure Prediction of Submodule Capacitors in Modular Multilevel Converter by Monitoring the Intrinsic Capacitor Voltage Fluctuations," *IEEE Trans. Ind. Electron.*, vol. 67, pp. 2585–2594, Apr. 2020.

[9] D. Ronanki and S. S. Williamson, "Quasi-online low-frequency impedance monitoring scheme for submodule capacitors in modular multilevel converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, pp. 83–90, 2019.

[10] X. Xin, Y. Yang, K. Ma, and B. He, "Online Monitoring for Sub-module Capacitance in Modular Multilevel Converter with Four Sampling Points of Capacitor Voltage," in *Proc. IEEE Int. Power Electron. Motion Control Conf.*, pp. 935–939, IEEE, Nov. 2020.

[11] Y.-J. Jo, T. H. Nguyen, and D.-C. Lee, "Condition monitoring of submodule capacitors in modular multilevel converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, pp. 2121–2126, 2014.

[12] F. Deng, Q. Wang, D. Liu, Y. Wang, M. Cheng, and Z. Chen, "Reference Submodule Based Capacitor Monitoring Strategy for Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 34, pp. 4711–4721, May 2019.

[13] C. Yin, F. Deng, Q. Yu, Y. Lv, Q. Heng, and Q. Wang, "Capacitor Monitoring for Full-Bridge Submodule Based Modular Multilevel Converters," in *Proc. Ind. Electron. Conf.*, pp. 3781–3786, IEEE, Oct. 2019.

[14] Z. Geng, M. Han, W. Xie, and T. Sun, "A Hierarchic Capacitor Condition Monitoring Strategy for High-Voltage Modular Multilevel Converters," *IEEE Trans. Power Syst.*, vol. 37, pp. 5310–5324, Dec. 2022.

[15] H. Wang, H. Wang, Z. Wang, Y. Zhang, X. Pei, and Y. Kang, "Condition Monitoring for Submodule Capacitors in Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 34, pp. 10403–10407, Nov. 2019.

[16] O. Abushafa, S. Gadoue, M. Dahidah, and D. Atkinson, "A new scheme for monitoring submodule capacitance in modular multilevel converter," in *Proc. 8th IET Int. Conf. Power Electron. Mach. Drives*, pp. 1–6, 2016.

[17] P. Venet, F. Perisse, M. El-Husseini, and G. Rojat, "Realization of a smart electrolytic capacitor circuit," *IEEE Ind. Appl. Mag.*, vol. 8, pp. 16–20, Feb. 2002.

[18] M. A. Vogelsberger, T. Wiesinger, and H. Ertl, "Life-Cycle Monitoring and Voltage-Managing Unit for DC-Link Electrolytic Capacitors in PWM Converters," *IEEE Trans. Power Electron.*, vol. 26, pp. 493–503, Feb. 2011.

[19] A. Gupta, O. P. Yadav, D. DeVoto, and J. Major, "A Review of Degradation Behavior and Modeling of Capacitors," in *Proc. Int. Tech. Conf. Exhib. Packag. Integr. Electron. Photon. Microsyst.*, pp. 1–10, American Society of Mechanical Engineers, Aug. 2018.

[20] B. Yao, S. Zhao, Y. Zhang, and H. Wang, "A health indicator of aluminum electrolytic capacitors based on strain sensing," *IEEE Trans. Power Electron.*, vol. 38, no. 7, pp. 7982–7987, 2023.

[21] H. Xia, Y. Zhang, M. Chen, W. Lai, D. Luo, and H. Wang, "Capacitor Condition Monitoring for Modular Multilevel Converter Based on Charging Transient Voltage Analysis," *IEEE Trans. Power Electron.*, vol. 38, pp. 3847–3856, Mar. 2023.

[22] F. Deng, Q. Heng, C. Liu, X. Cai, R. Zhu, Z. Chen, and W. Chen, "Capacitor ESR and C Monitoring in Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 35, pp. 4063–4075, Apr. 2020.

[23] H. Wang and F. Blaabjerg, "Reliability of Capacitors for DC-Link Applications in Power Electronic Converters—An Overview," *IEEE Trans. on Ind. Applicat.*, vol. 50, pp. 3569–3578, Sept. 2014.

[24] J. Stevens, J. Shaffer, and J. Vandenham, "The service life of large aluminum electrolytic capacitors: effects of construction and application," *IEEE Trans. Ind. Appl.*, vol. 38, no. 5, pp. 1441–1446, 2002.

[25] B. Yao, S. Zhao, Y. Zhang, and H. Wang, "A Health Indicator of Aluminum Electrolytic Capacitors Based on Strain Sensing," *IEEE Trans. Power Electron.*, vol. 38, pp. 7982–7987, July 2023.

[26] S. Du, A. Dekka, B. Wu, and N. Zargari, *Modular multilevel converters: analysis, control, and applications*. John Wiley & Sons, 2018.

[27] B. Wu and M. Narimani, *High-power converters and AC drives*. John Wiley & Sons, 2017.

[28] S. Du, J. Liu, and T. Liu, "Modulation and closed-loop-based dc capacitor voltage control for mmc with fundamental switching frequency," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 327–338, 2014.

[29] M. Clerc, *Particle Swarm Optimization*. London: ISTE, 1. publ ed., 2006.