

Pragmatic Formal Verification of Sequential Error Detection and Correction Codes (ECCs) used in Safety-Critical Design

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Abstract

Error Detection and Correction Codes (ECCs) are often used in digital designs to protect data integrity. Especially in safety-critical systems such as automotive electronics, ECCs are widely used and the verification of such complex logic becomes more critical considering the ISO 26262 safety standards. Exhaustive verification of ECC using formal methods has been a challenge given the high number of data bits to protect. As an example, for an ECC of 128 data bits with a possibility to detect up to four-bit errors, the combination of bit errors is given by $\binom{128}{4} + \binom{128}{3} + \binom{128}{2} + \binom{128}{1} \approx 1.1 \times 10^7$. This vast analysis space often leads to bounded proof results. Moreover, the complexity and state-space increase further if the ECC has sequential encoding and decoding stages. To overcome such problems and sign-off the design with confidence within reasonable proof time, we present a pragmatic formal verification approach of complex ECC cores with several complexity reduction techniques and know-how that were learnt during the course of verification. We discuss using the linearity of the syndrome generator as a helper assertion, using the abstract model as glue logic to compare the RTL with the sequential version of the circuit, k-induction-based model checking and using mathematical relations captured as properties to simplify the verification in order to get an unbounded proof result within 24 hours of proof runtime.

Index Terms

Formal Verification, Error Detection and Correction Code (ECC), k-Induction, Functional Safety (FuSa)

I. INTRODUCTION

Modern SoC designs are becoming more and more complex due to factors such as technology scaling, mixed-signal designs, safety and security-critical devices, more demand by customers from a single chip and many more. When such complex designs are made, one of the important aspect is to ensure data integrity. Especially in safety-critical systems and automotive electronics, the ISO 26262 functional safety standard plays a vital role to ensure the data loss is inevent. In a recent study done by the Wilson Research Group, 44 % of the Application-Specific Integrated Circuit (ASIC) projects are working on safety critical designs [1]. Another study from the same group in Fig. 1 shows that verification consumes approximately a median of 60 % of the overall project time. It can be depicted from the figure that the percentage of projects spending more than 50 % of their time in verification increased in 2022 compared to 2018. It becomes more evident that efficient methods of verification can be used in order to make sure that such safety critical designs are exhaustively verified. Formal verification is one such method that uses mathematical proofs to verify designs in a brute-force approach.

To protect the data against soft errors such as radiation errors, electrical glitches or electro-magnetic interference [2][3], there could be many possibilities of using safety measures such as dual/triple modular redundancy (DMR/TMR), ECC and alarm systems. However, the ECC serves as the better option over other measures since the efficiency is higher due to less redundant flops and consequently less area required for the chip. The ECC is also more flexible in terms of ability to distinguish between correctable and uncorrectable errors over other safety measures. In the context of functional safety, ISO 26262-5 also prescribes to use block replication or an ECC specifically for memories [4]. On the other hand, the complexity of ECC designs is rather high since there are lots of analysis-space and XOR gates. Conventionally, they are not formal friendly due to large vectors. Our paper is focused on overcoming the challenges of formal verification of such complex ECC designs.

II. BACKGROUND

A. Error Detection and Correction Code (ECC)

Error Detection and Correction Code (ECC) are used in digital designs to protect the data integrity. An ECC circuit consists of two stages, the first one is the ECC encoder and second one is the ECC decoder as shown in Fig. 2. The ECC encoder takes data input and computes the additional redundant bits called as ECC bits. The ECC bits are computed on two bases: the number of error bits to be detected and corrected, as well as the type of algorithm being used. Some of the algorithms such as Hamming Codes, Hsiao Codes, Reed-Solomon Codes and Bose-Chaudhuri-Hocquenghem Codes are commonly used encoding schemes for memory elements [5] [6]. The resulting output from the ECC encoder is a valid codeword that is written into

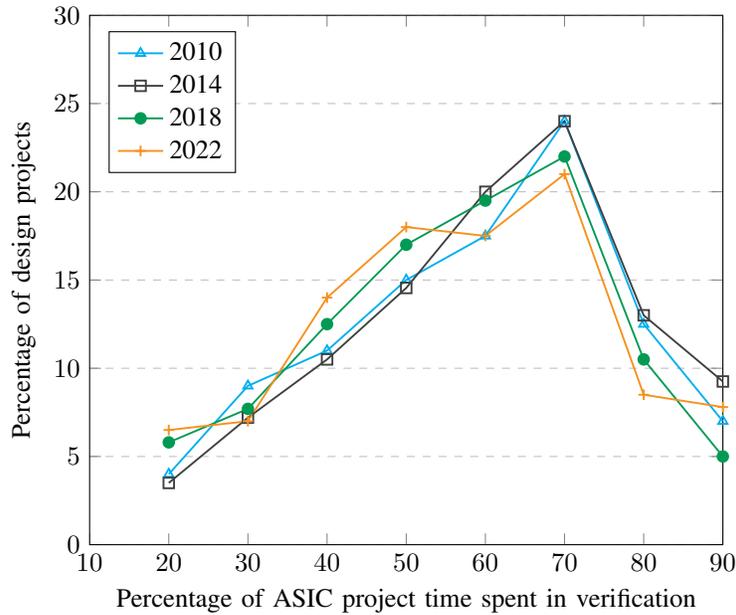


Fig. 1. Verification efforts required in overall product development [1]

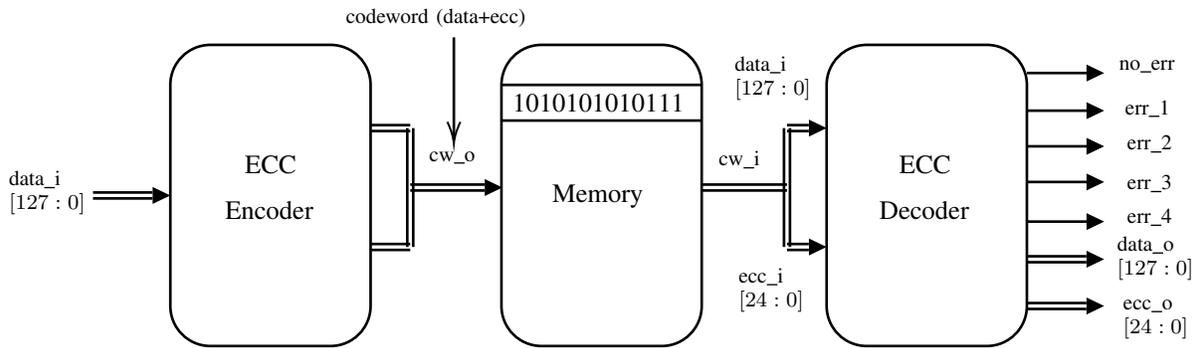


Fig. 2. ECC design with a memory

the memory. Some soft errors can occur in the memory due to factors such as radiation errors, electrical glitches or magnetic interference that could corrupt the codeword by a bit flip resulting in an invalid codeword. The output from the memory goes to the input of the ECC decoder as an invalid codeword and the ECC decoder detects the bit flips as well as correct them to send out valid/corrected data. The ECC used in this work is a combinatorial Quad Bit Error Detection, Triple Bit Error Correction (QEDTEC) ECC and later, a sequentially pipelined encoding/decoding stages is also used.

The existing approach uses simulation based verification with Specman-e testbench. The verification effort takes around 6 weeks to verify the ECC design. Even after several regression runs, the simulation based approach did not verify the design for all legal inputs which leads to a non brute-force approach of verification. As a result, the confidence on the design is low and not preferred for safety-critical designs. To overcome such issues, a formal based verification approach is used to exhaustively verify the correctness of the design.

B. Formal Verification

Formal verification uses technologies that mathematically analyze the space of possible behaviours of a design, rather than computing results for particular values [7]. It is an exhaustive verification technique that uses mathematical proof methods to verify whether the design implementation matches design specifications.

Fig. 3 shows the working of a formal verifier. There are two inputs to the formal verifier tool. On the one hand, the Design Under Verification (DUV) is fed into the tool and converted into a mathematical model. On the other hand, properties, written in SystemVerilog Assertions (SVA) that capture the intent of the design are also fed into the tool. The tool then converts these properties into mathematical formulas. In the next step, the tool tries to prove these mathematical formulas on the mathematical

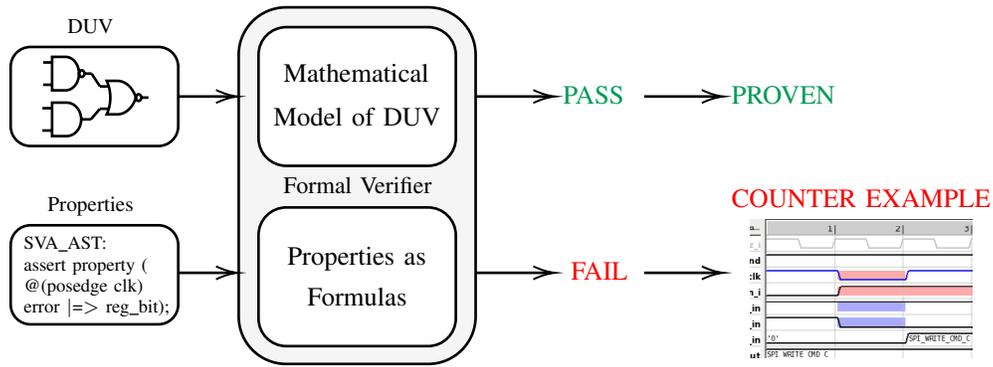


Fig. 3. Formal verifier [8]

model of the DUV. If the properties do not hold, it is said to be failed, and a Counter Example (CEX) is generated by the tool to debug further. In general, the absence of a CEX is a pass or proven result. Formal verification uses clever algorithms to verify the functional correctness of the design exhaustively [7]. However, for larger designs, it suffers state-space explosion and often takes longer than reasonable evaluation times for a conclusive proof result [7].

III. FORMAL VERIFICATION OF ECC

The motivation to use a formal based verification approach is to exhaustively verify that the design implementation matches the design specifications. However, since the ECC used in this work is a large design with a vast analysis space to cover, several complexity reduction techniques are used as well. To understand the formal verification, a step-wise approach is used and explained. At first, a verification plan is prepared as mentioned in the Fig. 4. Based on the verification plan, different properties are written to capture the intent of the design and prove the correctness.

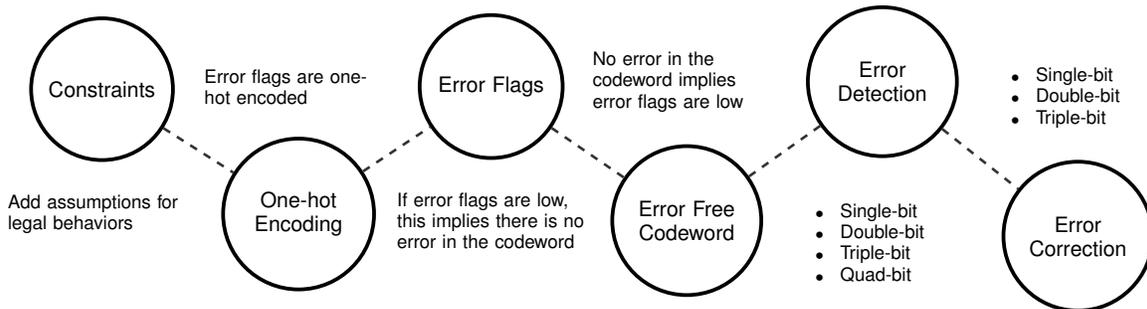


Fig. 4. Verification plan for ECC

A. Addressing Complexity Step 1: Remove Memory and Model Errors

The memory is irrelevant for proving the correctness of ECCs. In fact, memories are not very formal friendly and would increase the state-space, increase complexity as well as increase the proof time for the formal tool [9]. As a result, memory can be safely removed from the analysis space.

The next step is to model the errors in ECC codeword. For this purpose a SystemVerilog (SV) wrapper is prepared that instantiates the ECC encoder and the ECC decoder as shown in Fig. 5. The encoder outputs act as the primary outputs whereas the decoder inputs act as the primary inputs for the formal tool. As a result, the formal tool is free to take any possible values, unless constrained, for these primary inputs and outputs. The bit errors are introduced in the precondition of the properties written in SystemVerilog Assertions (SVA).

While preparing the properties to prove the correctness of the ECC, one of the requirements was to verify that exactly one of the error flags is high i.e., the error flags are one-hot encoded. Upon writing the property as mentioned in Listing 1, a bug was found where this requirement was violated. Although it was fixed in the design later, this already demonstrates how formal verification comes handy to expose simple bugs that could take more effort and time if verified using the conventional simulation based approach.

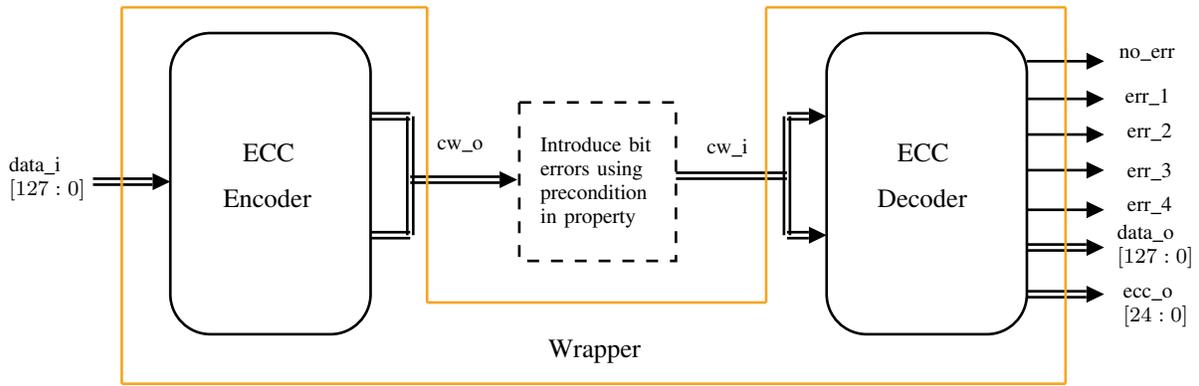


Fig. 5. Remove memory and model errors

```

1 //=====
2 // Prove that exactly one of the error flags is high i.e., one-hot encoding
3 //=====
4 property onehot_error_flags;
5     (1
6     |->
7     ( ($onehot({no_err, err_1, err_2, err_3, err_4})) );
8 endproperty
9 ap_onehot_error_flags : assert property(onehot_error_flags);

```

Listing 1. SVA property to prove error flags are one-hot encoded

In a standard brute-force approach, a SVA property to detect all 4 bit errors (multi bit errors) could be written as mentioned in Listing 2. The analysis space for the formal tool to prove the property in Listing 2 corresponds to $2^{128} \times \binom{153}{4}$ which is huge and results in an unbounded proof result.

```

1 //=====
2 // All multi bit errors (MBERR) shall be detected
3 //=====
4 property MBERR_detection;
5     ($countones(cw_o ^ cw_i) == 4)
6     |->
7     (err_4 && !err_1 && !err_2 && !err_3 && !no_err);
8 endproperty
9 ap_MBERR_detection : assert property(MBERR_detection);

```

Listing 2. SVA property to detect all multi bit errors

B. Addressing Complexity Step 2: The Linearity Approach

To address the complexity with large state-space, an attempt to explore the internals of the ECC decoder was made. The decoder primarily consists of three units: the syndrome generator, the error detection unit and the error correction unit as shown in Fig. 6. The syndrome generator computes the error syndrome for the codeword and is based on the encoding scheme used to generate the check bits [10]. The error detection unit sets the error flags and the error correction unit corrects the data in case of an invalid codeword based on the output from the syndrome generator.

The following observations were made for the syndrome generator:

- No error in codeword implies the syndrome output is a null vector.
- Syndrome generator is a linear function i.e., the syndrome output is independent of the data input.
- Syndrome output only depends on the erroneous bit positions.

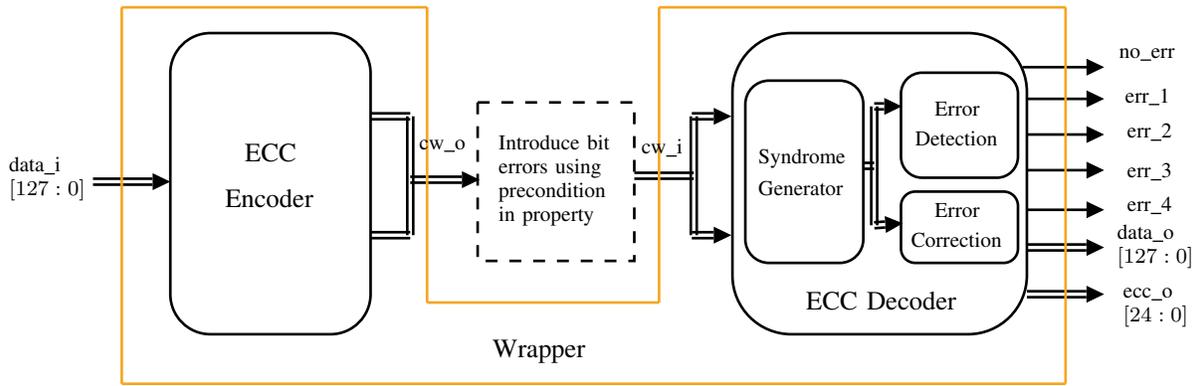


Fig. 6. Exploring ECC Decoder and its linearity

A function is an algebraic linear function if it preserves the addition operation, i.e., it satisfies the following mathematical rule:

$$f(x) + f(y) = f(x + y) \quad (1)$$

where x, y are arbitrary vector spaces. A linear function preserves the vector addition and scalar multiplication irrespective of the vector spaces and the scalar value [10]. Furthermore, the syndrome output is observed to be the erroneous bit position when a bit flip is introduced in the valid codeword. This is confirmed by noting the syndrom output for different codeword but same bit-error position as mentioned in Table I:

Codeword	Bit-Error Position	Syndrom Output
128'hcaba79a638aca501	6th bit position	25'd6
128'hec5e6af55ea3	6th bit position	25'd6
128'hcaba79a638aca501	18th bit position	25'd18
128'hec5e6af55ea3	18th bit position	25'd18

TABLE I

SYNDROME OUTPUT ONLY DEPENDS ON THE ERRONEOUS BIT POSITIONS

To prove the above three observations on the design, simple SVA properties could be written as stated in Listings 3, 4 and 5.

```

1 //=====
2 // Syndrome output of error free codeword is zero
3 //=====
4 property error_free_syndrome;
5     (cw_i == cw_o)
6     |->
7     (syn_o == 0);
8 endproperty
9 ap_error_free_syndrome : assert property(error_free_syndrome);

```

Listing 3. SVA property to prove syndrome output is a null vector for error free codeword

```

1 //=====
2 // Prove that syndrome generator is a linear function
3 //=====
4 property syndrome_linearity;
5     (syn(x) ^ syn(y) == syn (x ^ y));
6 endproperty
7 ap_syndrome_linearity : assert property(syndrome_linearity);

```

Listing 4. SVA property to prove syndrome generator is a liner function

```

1 //=====
2 // Syndrome output depends on the erroneous bit position
3 //=====
4 property error_bit_position;
5     (($countones(cw_o ^ cw_i) == 1) &&
6     (cw_o[6] != cw_i[6]))
7     |->
8     (syn_o == 6);
9 endproperty
10 ap_error_bit_position : assert property(error_bit_position);

```

Listing 5. SVA property to prove syndrome output only depends on the erroneous bit position

Proving linearity means the syndrome output is independent of the data input. These helper asserts will be proven and therefore implicitly assumed for improved proof performance of other properties. Since the data input does not contribute to the syndrome output, the multi bit error detection can now be further simplified to use a randomly selected fixed data input and prove the property as shown in Listing 6. Similarly, a SVA property to prove 3 bit error correction could be written as Listing 7. The reduced analysis space for the formal tool to prove the property in Listing 6 is $1x \binom{153}{4}$ and the proof time is 10 hours.

```

1 //=====
2 // All multi bit errors (MBERR) shall be detected
3 //=====
4 property MBERR_detection;
5     ((data_i == 128'hcaba79a638aca501) // random
6     && ($countones(cw_o ^ cw_i) == 4))
7     |->
8     (err_4 && !err_1 && !err_2 && !err_3 && !no_err);
9 endproperty
10 ap_MBERR_detection : assert property(MBERR_detection);

```

Listing 6. SVA property to to detect all multi bit errors together with linearity approach

```

1 //=====
2 // All triple bit errors (TBERR) shall be corrected
3 //=====
4 property TBERR_correction;
5     ((data_i == 128'hcaba79a638aca501) &&
6     ($countones(cw_o ^ cw_i) == 3) && (err_3))
7     |->
8     ((dec_data_o == enc_data_i) && (dec_ecc_o == enc_ecc_o));
9 endproperty
10 ap_TBERR_correction : assert property(TBERR_correction);

```

Listing 7. SVA property to to correct all 3 bit errors together with linearity approach

C. Addressing Complexity Step 3: Using Reduced Latency Model

A sequential version of the ECC core is also verified using the formal approach as shown in the Fig. 7. The core has a sequentially pipelined encoding and decoding stages.

Fig. 8 shows the timing diagram of the sequential ECC core having 6 clock cycles for encoding, 3 clock cycles for error detection and 2 additional clock cycles for error correction. Upon applying the linearity approach, the formal tool gave up after 120 hours with a bounded proof result.

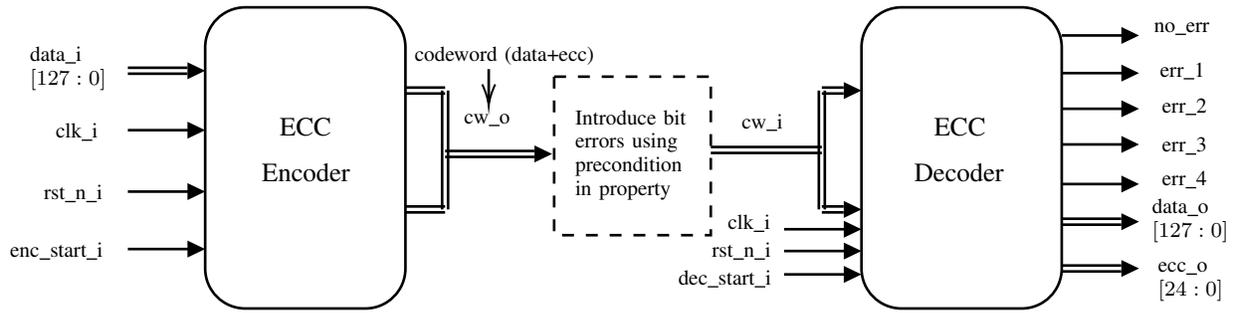


Fig. 7. Sequential ECC core

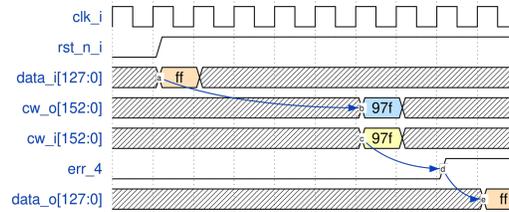


Fig. 8. Timing diagram of sequential ECC core

It is evident that the encoder has a longer latency in terms of the clock cycles. This in turn increases the state-space for the formal tool and requires more proof time. To overcome this challenge, a cycle inaccurate model of the ECC encoder is prepared in a combinational SystemVerilog function. The model calculates the the ECC bits in the same clock cycle based on the Reed-Solomon code (as used in the design). In order to prove the correctness of the model, an equivalence check between the combinational function and the sequential encoding output from the RTL design is performed by assuming equal inputs for both and comparing the outputs at the end as shown in Fig. 9. The SVA property to prove the equivalence is mentioned in the Listing 8.

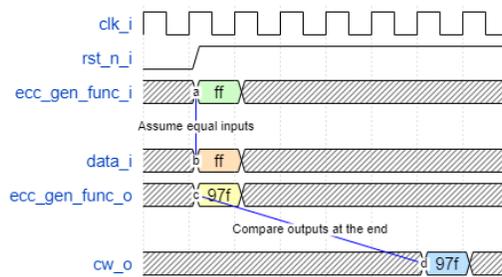


Fig. 9. Comparing model against the RTL

```

1 //=====
2 // Prove equivalence between RTL and model
3 //=====
4 property equivalence;
5     (data_i == 128'hcaba79a638aca501)
6     |->
7     ##5 ({ecc_gen_func(data_i), data_i}) == cw_o);
8 endproperty
9 ap_equivalence : assert property (@(posedge clk) disable iff (!rst_n) equivalence);

```

Listing 8. SVA property to prove the equivalence between RTL and the cycle inaccurate model

The model is used afterwards in the properties as a glue logic to prove the correctness of the design.

D. Addressing Complexity Step 4: Use SST Traces to Help with Induction-Based Proof

For sequentially deep designs such as the sequential ECC used in this work, it might get difficult to get an unbounded proof result within reasonable time. In spite of using the above mentioned complexity reduction techniques, a few properties such as the 4 bit error correction struggles to prove. To overcome this problem, an induction-based proof method or k-induction is used. Induction is a method to check if the design is in a random good state whether it will be in a good state at the next cycle [11]. k-induction bounded model checking consists of two steps. These are the base case and the induction step [12]. To begin, rather than just one state, the property is assumed to hold for a path of n successive states. This means that a more extensive base-case must be demonstrated. Second, the path's states are assumed to be distinct. Finiteness implies that the second strengthening completes the method in the sense that there is always a length for which the induction-step is provable [13]. This can be formalized as equations (2) and (3) [13]:

$$\text{Base}_n := I_0 \wedge ((P_0 \wedge T_0) \wedge \dots \wedge (P_{n-1} \wedge T_{n-1})) \wedge \overline{P_n} \quad (2)$$

$$\text{Step}_n := ((P_0 \wedge T_0) \wedge \dots \wedge (P_n \wedge T_n)) \wedge \overline{P_{n+1}} \quad (3)$$

where I_0 is the initial state, P_0 is the property in initial state and T_0 is time zero. n is the time step. The interpretation of these formulas/equations is mentioned in Fig. 10. If the n -th base-case is unsatisfiable, the statement should be interpreted as “There exists no n -step path to a state violating the property, assuming the property holds the first $n-1$ steps”. If the n -th induction-step is unsatisfiable, it should be read as “Following an n -step trace where the property holds, there exists no next state where it fails”. SAT solvers are used in modern EDA tools to solve such induction equations.

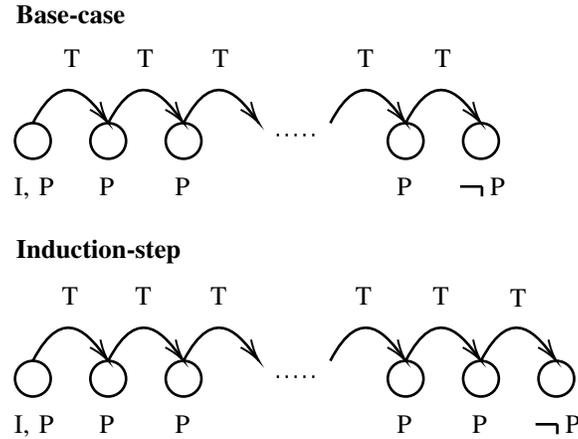


Fig. 10. Base-case and induction-step [13]

In a simple and abstract explanation to understand proof using induction, assume the equations (4) and (5) about a design:

$$A_1 = 1 \quad (4)$$

$$(A_n \rightarrow A_{n+1}) = 1 \quad (5)$$

Step (4) is proving whether the assertion holds true for the 1st clock cycle and step (5) checks to prove whether the assertion A holds true on a random state A_n which would mean it will hold true for the next clock cycle (A_{n+1}) as well. If step (4) and (5) are true, this proves that A is true for all clock cycles [11].

Modern EDA tools such as Cadence JasperGold offer solutions like the State-Space Tunneling (SST) based on induction-based proof where a systematic process is used to reduce the state space of a target property. The reduction is essentially done by identifying such states and writing helper assertions called as lemmas. Helper assertions are properties about internal signals (states) in the design that, if proven, will be used as “assumptions” in the proof process of the target property (or other properties), allowing these proven properties to aid in the elimination of states [11]. An SST trace is a normal Counter Example (CEX) of the property, but since it does not start at reset states, this trace exemplifies the target property failure [11]:

- For a true property, this trace starts from an unreachable good state and ends outside the property in a bad state.
- For a false-property, the trace can start from reachable good state and end in reachable bad state.

As the SST process normally focuses on true properties, the trace is a normal CEX that starts at an unreachable state, continues for $N-1$ cycles in unreachable states, then violates the target property on the last cycle. These SST traces helps to write the helper assertions. Additionally, the SST process provides a deeper understanding of the design and relationships that exist between its state variables. This deeper understanding can help the user tune the model and/or prove other properties beyond the target property [11]. A usual SST based flow is depicted in Fig. 11.

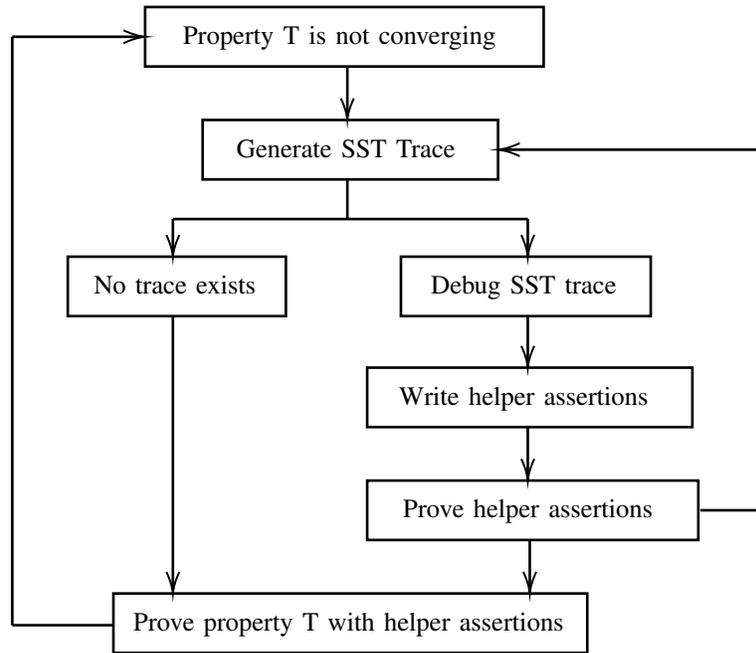


Fig. 11. k-Induction and SST based verification flow [11]

While analyzing the SST trace for the ECC design, two issues were found in the violation due to missing constraints:

- The decoder FSM should start from IDLE state when decoding starts (Fig. 12).
- Decoding should start only after encoding is finished (Fig. 13).

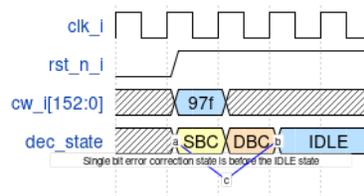


Fig. 12. Decoder FSM did not start from IDLE state when decoding starts

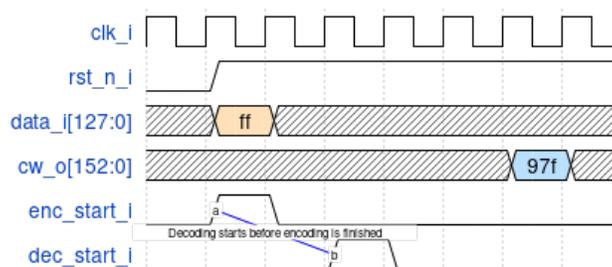


Fig. 13. Decoding starts before encoding is finished

As a result the induction steps fail for increasingly longer paths, contributing towards longer proof runtime. After adding these two missing constraints in Listings 9 and 10, all the properties proved within 24 hours.

```

1 //=====
2 // Assume that the decoder is in IDLE state when decoding is started
3 //=====
4 property dec_idle_state;
5     ( (dec_start_i)
6     |->
7     ( dec_state == IDLE ));
8 endproperty
9 cp_dec_idle_state : assume property(dec_idle_state);

```

Listing 9. SVA property to assume that the decoder starts from the IDLE state

```

1 //=====
2 // Assume that encoding and decoding do not overlap
3 //=====
4 property no_overlap;
5     ( (enc_start_i)
6     |->
7     ( !dec_data_valid_i ) [*5] );
8 endproperty
9 cp_no_overlap : assume property(@(posedge clk) disable iff (!rst_n) no_overlap);

```

Listing 10. SVA property to assume that encoding and decoding stages do not overlap

IV. CONCLUSION AND FUTURE WORK

ECCs are commonly used safety mechanism to ensure the functional safety. An exhaustive verification of such safety-critical design is very important. A pragmatic formal verification approach for complex ECC designs is presented in this paper. Several ECC cores with combinatorial and sequentially pipelined encoding/decoding stages are verified using the proposed approach. The linearity of the syndrome generator is used to limit the input data to a reasonable analysis space and make the design formal-friendly. An equivalent cycle inaccurate model for sequential ECCs is used to reduce the latency for the formal tool and prove the properties in less proof time. During the course of verification, some design bugs such as incorrect one-hot encoding of the error flags were unveiled and fixed before the tape-out. It may be noted that for different formal tools, selection and tuning of the appropriate engine settings also plays an important role. Since EDA tools are becoming more advanced and deploy different engines to solve specific mathematical problems related to the properties, a right set of engines also helps in a faster proof time. For the ECC verified in this paper, it took 24 hours to prove all the properties together with the complexity reduction techniques discussed whereas, it took 18 hours to prove the properties with dedicated engine settings.

Although the proposed verification method is scalable and works on standard ECC designs, it is noted that the designs having higher data width, or higher number of bits to detect and correct, or higher latency in encoding/decoding stages, or all of them, make the tool suffer to give an unbounded proof result within reasonable time. As a future work, one could look into the possibility of using even better abstract models such as C/C++/SystemC and use software based formal verification tools such as CBMC [14] or ESBMC [15] to prove the properties by exploiting word-level nature of C/C++ and speedup the verification process. Later on, an equivalence check between the RTL and the abstract model could be done to prove the correctness of the design.

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