

Resource-compact time-optimal quantum computation

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Abstract

Fault-tolerant quantum computation enables reliable quantum computation but incurs a significant overhead from both time and resource perspectives. To reduce computation time, Austin G. Fowler proposed time-optimal quantum computation by constructing a quantum circuit for a fault-tolerant T gate without probabilistic S gate correction. In this work, we introduce a resource-compact quantum circuit that significantly reduces resource requirements by more than 60% for a fault-tolerant T gate without probabilistic S gate correction. Consequently, we present a quantum circuit that minimizes resource utilization for time-optimal quantum computation, demonstrating efficient time-optimal quantum computation. Additionally, we describe an efficient form involving initialization, CNOTs, and measurements, laying the foundation for the development of an efficient compiler for fault-tolerant quantum computation.

1 Introduction

Fault-tolerant quantum computing [1, 2, 3] is necessary for reliable computation in real-world environments. Overcoming errors and ensuring the reliability of quantum computations are critical steps towards achieving the transformative capabilities promised by quantum computing technology. Fault-tolerant quantum computation imposes significant resource demands, encompassing the need for additional qubits, increased circuit depth, ancillary qubits, and computational overhead for error correction. Addressing these challenges is essential for advancing the field of quantum computing system software and realizing the full potential of fault-tolerant quantum algorithms in practical applications. Thus, it is necessary to reduce the resources required to run fault-tolerant quantum computation as much as possible. For this purpose, several studies have been conducted and are still in progress [4, 5, 6, 7, 8].

In fault-tolerant quantum computation, error correction and feedforward processes were believed to cause considerable time overhead, highlighting a key limitation in efficiency. However, it is known that such overhead can be significantly reduced by a circuit that can perform T gates without applying S gate correction probabilistically [9]. Thus, given a quantum error-correcting code that enables universal fault-tolerant quantum computation and transversal measurement of logical X and Z , the methodology for executing *time-optimal quantum computation* has been proposed. This means that the asymptotic time complexity of the arbitrary quantum algorithm execution corresponds to the product of the number of layers consisting of independent T gates and a single physical measurement time. In other words, surprisingly, it was demonstrated that the number of independent T gates can determine the overall execution speed of quantum computation, highlighting its importance [8, 10, 11, 12, 13].

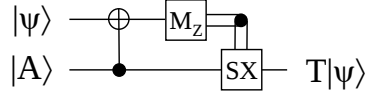


Figure 1: Quantum circuit for fault-tolerant T gate with probabilistic S gate correction [15].

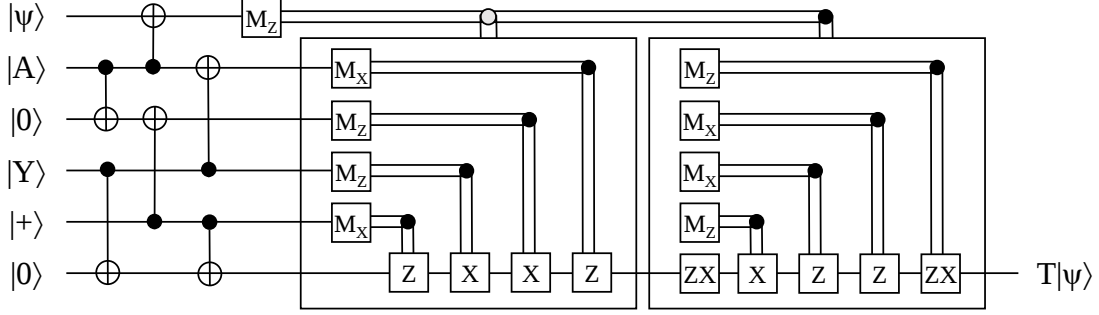


Figure 2: Quantum circuit for fault-tolerant T gate without probabilistic S gate correction [9].

On the other hand, arbitrary fault-tolerant quantum computation can be converted into the Initialization, CNOT, and Measurement form [14]. The form is called *ICM form*. It is known that the form allows a more flexible approach towards circuit optimization for an appropriate compiler to produce a fault-tolerant, error-corrected description from a higher-level quantum circuit. The ICM form is composed based on the previous known circuit for fault-tolerant implementation for the T gate [9].

The previous known circuit for fault-tolerant T gate implementation is based on selective destination teleportation and selective source teleportation. Thus, the circuit requires more resources than are absolutely necessary to perform it. In this work, we design a circuit that directly performs fault-tolerantly T gate without selective destination teleportation and selective source teleportation in order to design a more efficient circuit. Utilizing our circuit design for a fault-tolerant T gate, we demonstrate time-optimal quantum computation with minimized resources and describe the ICM form, also optimized in terms of resources.

2 Quantum circuits for a fault-tolerant T gate

An arbitrary fault-tolerant quantum computation can be performed using only controlled- NOT , H , S , and T gates [15]. Generally, it has been turned out to be very simple to implement the controlled- NOT , H , and S gates fault-tolerantly. In order to complete the set of gates for universal quantum computation, it is necessary to perform the T gate in a fault-tolerant manner.

A quantum circuit implementing fault-tolerantly a T gate is shown in Figure 1. Here, $|A\rangle = TH|0\rangle$. The state $|A\rangle$ can be prepared either directly via state distillation [16]. In the circuit, the measurement is performed in the first qubit, and if the measurement result is 0 then it is done. Otherwise, the operation SX is performed to the second qubit. In other words, based on the measurement results, the S gate is applied probabilistically.

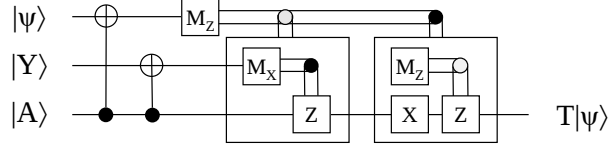


Figure 3: Our quantum circuit for fault-tolerant T gate without probabilistic S gate correction.

A quantum circuit for a fault-tolerant T gate without a probabilistic S gate correction can be performed by the combination of selective destination teleportation, selective source teleportation and the circuit for a fault-tolerant T gate in Figure 1. Figure 2 shows a quantum circuit implementing a T gate without a probabilistic S gate correction [9]. Here, $|Y\rangle = SH|0\rangle$ and $|+\rangle = H|0\rangle$. The circuit shown in Figure 2 is slightly modified using circuit identity to reduce depth. To ensure that the T gate is performed accurately, we have calculated operations based on the measurement results and included them in the Figure 2. From the circuit depicted in the Figure 2, we can deduce the following Proposition 1.

Proposition 1. *A quantum circuit to perform a T gate without probabilistically applying the S gate can be designed using a maximum of 5 ancillary qubits, 6 CNOTs and 5 X - or Z -basis measurements [9].*

Since $|Y\rangle = SH|0\rangle$, the S gate is included in the process of generating the $|Y\rangle$ state and is applied deterministically, not probabilistically. In the circuit in Figure 2, operations based on measurement results are performed using only the X or Z gate. Thus, performing X or Z gates followed by Clifford gates can be converted to performing Clifford gates first and then performing X or Z gates appropriately. It can be used to parallelize quantum circuits.

Constructing a quantum circuit for a fault-tolerant T gate without employing probabilistic S gate correction via selective destination and source teleportation may seem intuitively straightforward. However, we design a circuit that directly performs fault-tolerantly T gate without selective destination and selective source teleportation in order to design a more efficient circuit. Figure 3 shows our circuit. The circuit utilizes only two ancillary states, represented as $|Y\rangle$ and $|A\rangle$. The circuit necessitates 2 CNOT operations and also requires 2 measurements in either the X - or Z -basis. Therefore, from the circuit depicted in the Figure 3, we can deduce the following Theorem 1.

Theorem 1. *A quantum circuit to perform a T gate without probabilistically applying the S gate can be designed using a maximum of 2 ancillary qubits, 2 CNOTs and 2 X - or Z -basis measurements.*

The proof can be established through straightforward calculations. However, we elaborate on the proof to demonstrate the correctness of our circuit in implementing the T gate.

Proof. Let $|\psi\rangle = \alpha|0\rangle + \beta|1\rangle$, where $|\alpha|^2 + |\beta|^2 = 1$. Then,

$$\begin{aligned} |\psi\rangle |Y\rangle |A\rangle &= \frac{1}{2}(\alpha|000\rangle + e^{\frac{\pi i}{4}}\alpha|001\rangle + i\alpha|010\rangle + ie^{\frac{\pi i}{4}}\alpha|011\rangle \\ &\quad + \beta|100\rangle + e^{\frac{\pi i}{4}}\beta|101\rangle + i\beta|110\rangle + ie^{\frac{\pi i}{4}}\beta|111\rangle). \end{aligned} \quad (1)$$

Thus,

$$\begin{aligned} CNOT_{32}CNOT_{31}|\psi\rangle |Y\rangle |A\rangle &= \frac{1}{2}(\alpha|000\rangle + e^{\frac{\pi i}{4}}\alpha|111\rangle + i\alpha|010\rangle + ie^{\frac{\pi i}{4}}\alpha|101\rangle \\ &\quad + \beta|100\rangle + e^{\frac{\pi i}{4}}\beta|011\rangle + i\beta|110\rangle + ie^{\frac{\pi i}{4}}\beta|001\rangle). \end{aligned} \quad (2)$$

resources	the previous circuit	our circuit
number of ancillary qubits	5	2
number of $CNOT$ s	6	2
number of measurements	5	2

Table 1: Comparison between the previous circuit and our circuit for fault-tolerant T gate implementation. Reduction rates: Ancillary qubits - 60%, $CNOT$ s - 67%, Measurements - 60%.

Next, a Z -basis measurement is performed on the first qubit, and depending on the measurement result of the first qubit, X -basis measurement or Z -basis measurement is performed on the second qubit. Let us denote the outcome of the Z -basis measurement result on the first qubit as m_{Z_1} . Let us denote the outcome of $X(Z)$ -basis measurement result on the second qubit as $m_{X_2}(m_{Z_2})$.

1. If $m_{Z_1} = 0$, then $\frac{1}{\sqrt{2}} |0\rangle (\alpha |00\rangle + i\alpha |10\rangle + e^{\frac{\pi i}{4}} \beta |11\rangle + ie^{\frac{\pi i}{4}} \beta |01\rangle)$.

(a) If $m_{X_2} = 0$, then $\frac{1+i}{\sqrt{2}} |0\rangle |+\rangle T_3 |\psi\rangle$.

(b) If $m_{X_2} = 1$, then $\frac{1-i}{\sqrt{2}} |0\rangle |-\rangle (\alpha |0\rangle - e^{\frac{\pi i}{4}} \beta |1\rangle)$.

Therefore, $\frac{1-i}{\sqrt{2}} |0\rangle |-\rangle Z_3(\alpha |0\rangle - e^{\frac{\pi i}{4}} \beta |1\rangle) = \frac{1-i}{\sqrt{2}} |0\rangle |-\rangle T_3 |\psi\rangle$.

2. If $m_{Z_1} = 1$, then $\frac{1}{\sqrt{2}} |1\rangle (e^{\frac{\pi i}{4}} \alpha |11\rangle + ie^{\frac{\pi i}{4}} \alpha |01\rangle + \beta |00\rangle + i\beta |10\rangle)$.

(a) If $m_{Z_2} = 0$, then $|10\rangle (ie^{\frac{\pi i}{4}} \alpha |1\rangle + \beta |0\rangle)$.

Therefore, $|10\rangle Z_3 X_3 (ie^{\frac{\pi i}{4}} \alpha |1\rangle + \beta |0\rangle) = ie^{\frac{\pi i}{4}} |10\rangle T_3 |\psi\rangle$.

(b) If $m_{Z_2} = 1$, then $|11\rangle (e^{\frac{\pi i}{4}} \alpha |1\rangle + i\beta |0\rangle)$.

Therefore, $|11\rangle X_3 (e^{\frac{\pi i}{4}} \alpha |1\rangle + i\beta |0\rangle) = e^{\frac{\pi i}{4}} |11\rangle T_3 |\psi\rangle$.

□

Table 1 presents a comparison between the previously known circuit and our proposed circuit for implementing the fault-tolerant T gate. For fault-tolerant quantum computation employing n independent T gates, the previous circuit necessitates $5n$ ancillary qubits, whereas our circuit requires only $2n$. Consequently, relative to the prior approach, the ratio of ancillary qubits required in the circuit can be reduced by 60%. The number of $CNOT$ s and number of measurements for fault-tolerant quantum computation can also be reduced significantly. Furthermore, operations based on measurement results are considerably simpler than those of previous circuits.

A circuit for a fault-tolerant T gate appears that a minimum of two ancillary qubits are essential for deterministic fault-tolerant implementation of the T gate without probabilistic S gate correction. One corresponds to the state $|A\rangle$ for the application of the T gate, while the other relates to the state $|Y\rangle$ intended for the S gate application. Each of these ancillary qubits seemingly necessitates at least one two-qubit gate to entangle with a given state $|\psi\rangle$. Thus, configuring a quantum circuit for fault-tolerant T gate implementation appears challenging, particularly when aiming for further resource reduction compared to our circuit, especially under the same conditions where measurements and operations depending on the measurement results.

In a similar way, a quantum circuit for fault-tolerant $T^\dagger$ gate implementation can be obtained as shown in Figure 4. The structure of a quantum circuit for fault-tolerant $T^\dagger$ gate implementation is similar to a structure of a quantum circuit for fault-tolerant T gate implementation.

time.

Utilizing our proposed design, the circuit $(HT)^n$ can be more efficiently constructed, as depicted in Figure 5 (b). It consists of $2n$ ancillary qubits, n CNOTs, n CZ, 2 H s and $2n$ X - or Z -basis measurements. The circuit depth encompasses a depth of 3 for the Clifford circuit and an additional depth of $n + 1$ for measurements, resulting in a total depth of $n + 4$ excluding X or Z gates based on measurement results. The ratio of ancillary qubits needed for the fault-tolerant $(HT)^n$ circuit has decreased by 60%, from $5n$ to $2n$. Although the ratio of CZs required is the same at n , the ratio of CNOTs has decreased by 80% from $5n$ to n . The ratio of measurements required has also decreased by 60%, from $5n$ to $2n$.

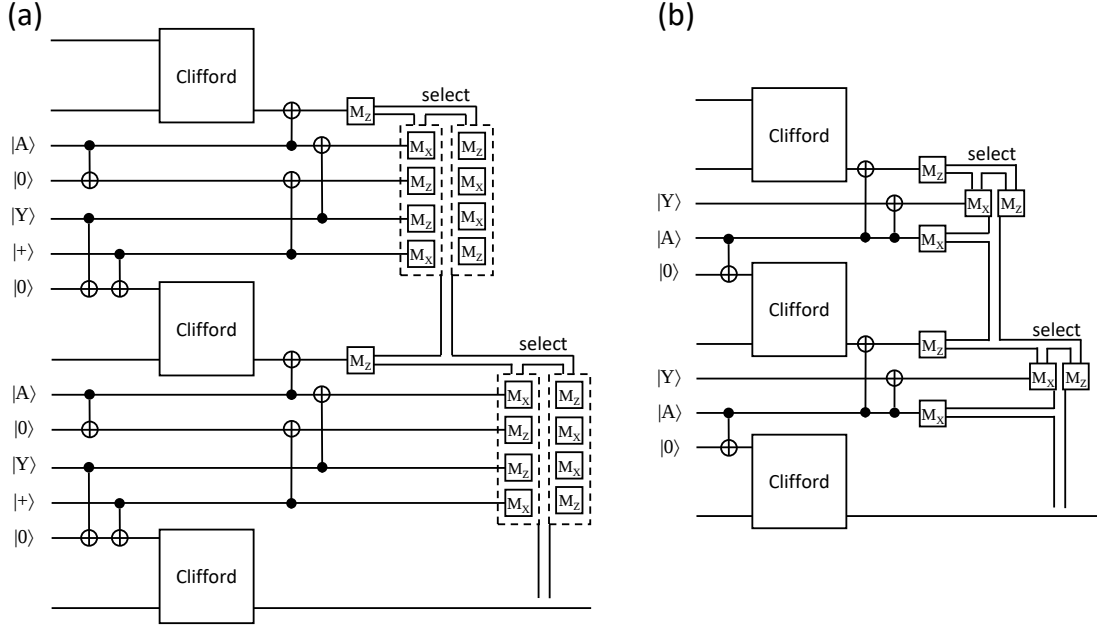


Figure 6: Time-optimal quantum computation: (a) Using the previous known circuit (b) Using our circuit. Reduction rates: Ancillary qubits - 40%, CNOTs - 50%, Measurements - 40%.

In general, arbitrary quantum computations can be consisted of Clifford gates and T gates. The circuit in the Figure 6 (a) can be obtained by using the previous circuit for fault-tolerant T gate implementation. The circuit consists of parallel Clifford gates including CNOTs for T gate implementation and time-ordered X - or Z -basis measurements. This is known as *time-optimal quantum computation*.

Utilizing our proposed design, the circuit can be more efficiently constructed, as depicted in Figure 6 (b). For each fault-tolerant T gate implementation, the number of ancillary qubits required is only 2. However, to parallel Clifford gates, gate teleportation is additionally performed. Thus, one additional ancillary qubit is used for each T gates. Even considering parallel Clifford gates, the ratio of ancillary qubits required for time-optimal quantum computation is reduced by 40%. If parallel Clifford gates are not considered, quantum computation is possible with fewer resources because gate teleportation is not required. The following Corollary 1 can be obtained.

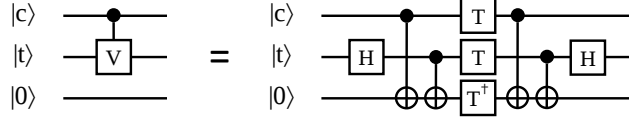


Figure 7: Our decomposition of the controlled- V gate employing an ancillary qubit.

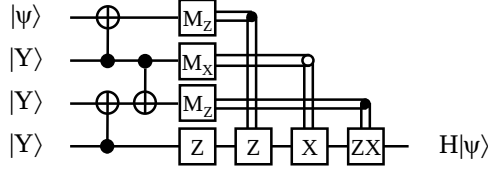


Figure 8: ICM form for the H gate [17].

Corollary 1. *Arbitrary quantum computation can be transformed into a quantum circuit for time-optimal quantum computation using a maximum of 3 ancillary qubits, 3 CNOT operations, 3 measurements in either the X - or Z -basis, and solely X or Z operations depending on the measurement results for each independent T gate.*

As evident from the Corollary 1, executing fault-tolerant quantum computation expeditiously is feasible with fewer resources compared to existing methods.

4 Efficient ICM form

Arbitrary quantum computation can be converted into the Initialization, CNOT, and Measurement form [14]. First, the initialization layer of qubits consists of one of four distinct states ($|0\rangle$, $|+\rangle$, $|Y\rangle$, $|A\rangle$). Secondly, the CNOT layer consists of a massive and deterministic array of CNOT operations. Last, the measurement layer consists of a series of time-ordered X - or Z -basis measurements. The ICM form facilitates a versatile methodology for circuit optimization. Concurrently, the package yields either a standard circuit or a canonical geometric description, essential for interfacing with contemporary hardware architectures that employ topological quantum codes.

As a simple example, a controlled- V gate can be converted into the ICM form. First of all, the controlled- V gate can be decomposed into 2 H s, 4 CNOTs, 2 T s and 1 $T^\dagger$ with an ancillary qubit as shown in Figure 7. Through simple calculations, the H gate can be converted into the ICM form as shown in Figure 8 [17]. By using the previous circuit for the implementation of the T gate, circuit shown in Figure 9 (a) can be obtained. It consists of 22 ancillary qubits, 28 CNOTs and 21 X - or Z -basis measurements. By employing our circuit for T gates depicted in Figure 3 and the circuit for $T^\dagger$ gates shown in Figure 4, the form can be designed with reduced resources. The ICM form for the controlled- V gate is illustrated in Figure 9 (b). It consists of 13 ancillary qubits, 16 CNOTs and 12 X - or Z -basis measurements. Therefore, it can be seen that all resources are reduced by more than 40% compared to using a circuit in Figure 9 (a). Consequently, it can facilitate the development of an efficient compiler for fault-tolerant quantum computation.

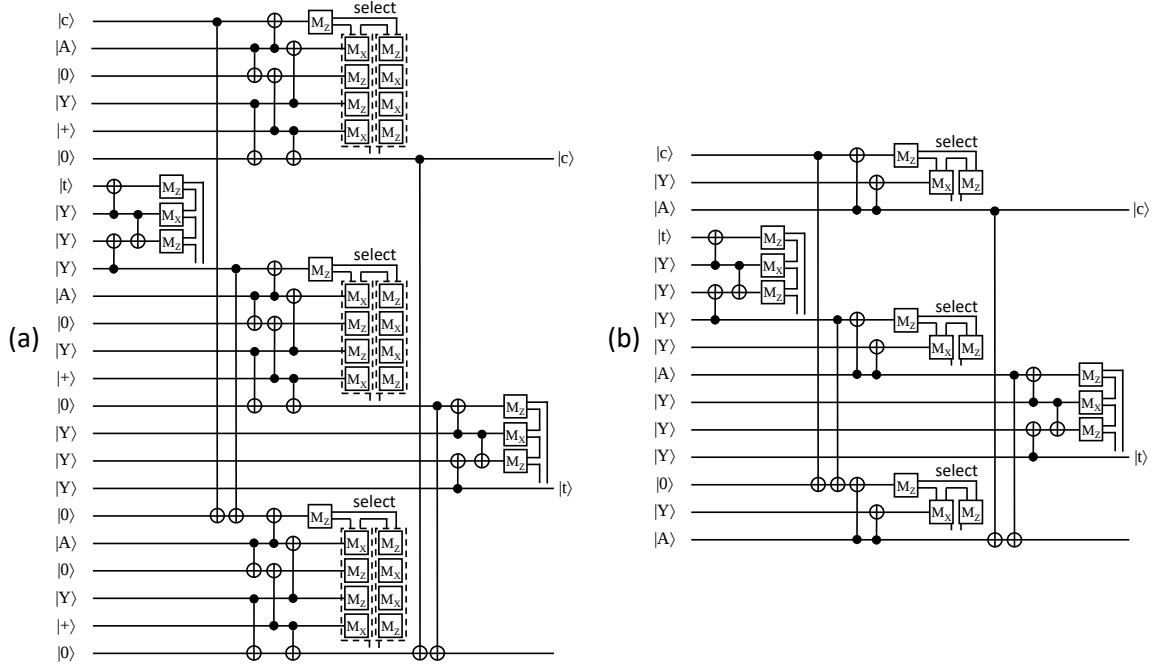


Figure 9: ICM form of the controlled-V gate: (a) ICM form using the previous known circuit for the controlled-V gate. (b) Our ICM form utilizing our circuit for the controlled-V gate. Reduction rates: Ancillary qubits - 41%, CNOTs - 43%, Measurements - 43%.

5 Conclusion

We have explored the expeditious execution of fault-tolerant quantum computation while minimizing resource consumption. We have presented a quantum circuit that significantly reduces resource requirements by more than 60% for a fault-tolerant T gate without probabilistic S gate correction. Our circuit exhibits a 60% reduction in ancillary qubits, a 67% reduction in CNOT gates, and a 60% reduction in measurements. Consequently, we have presented a quantum circuit that minimizes resource utilization for time-optimal quantum computation, demonstrating efficient time-optimal quantum computation with over 40% reduced resources. Specifically, ancillary qubits are reduced by 40%, CNOT gates by 50%, and measurements by 40%. Additionally, we have described the efficient ICM form for development of a compiler for fault-tolerant quantum computation.

The efficiency of our circuit has been attained by directly configuring the circuit without relying on selective destination teleportation and selective source teleportation while attempting to implement a fault-tolerant T gate without probabilistically applying the S gate. Configuring a quantum circuit for fault-tolerant T gate implementation appears challenging, especially when aiming for further resource reduction compared to our circuit under the same measurement conditions.

Our study emphasizes a significant enhancement in the efficiency of fault-tolerant T gate implementation. The circuit holds potential for contributing to the advancement of quantum computing system software, such as the development of an efficient compiler for fault-tolerant quantum computation.

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