

Anomalous Gate-tunable Capacitance in Graphene Moiré Heterostructures

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Abstract

Interface engineered ferroelectricity in van der Waals heterostructures is of broad interest both fundamentally and technologically for the applications in neuromorphic computing and so on. In particular, the moiré ferroelectricity in graphene/hexagonal boron nitride (hBN) heterostructures driven by charge ordering instead of traditional lattice displacement has drawn considerable attention because of its fascinating properties and promising high-frequency programmable electrical polarization switching. Yet, the underlying mechanism of the electronic ferroelectricity is still under debate. On the other hand, combining the interface engineered ferroelectricity and strong correlations in moiré heterostructures could enable the realization of novel quantum states such as ferroelectric superconductivity and multiferroicity. Here we study the electronic transport properties of twisted double bilayer graphene (TDBLG), aligned with one of the neighbouring hBN. We observe a strong gating hysteresis and ferroelectric-like behaviour, as well as the electronic ratchet effect. We find that the top gate is anomalously screened. On the contrary, the back gate is anomalously doubly efficient in injecting charges into graphene, that is, the effective back gate capacitance is two times larger than its geometry capacitance. This unexpected gate-tunable capacitance causes a dramatic change of electric fields between forward and backward scans. The asymmetric gating behaviours and anomalous change in capacitance could be explained with a simple model involved with a spontaneous electric polarization between top hBN and graphene. Our work provides more insights into the mysterious ferroelectricity in graphene/hBN moiré heterostructures and paves the way to the understanding of the underlying mechanism.

Two-dimensional (2D) ferroelectricity with spontaneous electric polarization is not only fundamentally interesting in physics, but also technologically important towards the goal of device miniaturization and the non von Neumann computing architectures. Of particular interest is the interface engineered ferroelectricity in van der Waals heterostructures composed of non-polar 2D materials such as graphene and hBN, where the electric polarization switching is induced by the interlayer sliding. Such sliding ferroelectricity has been predicted and verified in van der Waals bilayers of hBN, transition metal dichalcogenides (TMDc) and many other van der Waals materials[1–10]. Moreover, aligned graphene/hBN heterostructures[11–14] provide one of the rare systems where moiré ferroelectricity is driven by charge ordering instead of conventional ionic displacement. The electronic ferroelectricity is promising for high-frequency electrical polarization switching and neuromorphic transistors[15,16]. Despite its fascinating properties and potential

applications, the underlying mechanism of electronic ferroelectricity in aligned graphene/hBN heterostructures remains to be uncovered.

On the other hand, moiré engineering is an effective approach to create novel quantum states arising from strong electronic correlations. For instance, the interface hybridization between two twisted graphene layers near the magic angle of 1.1° would quench the kinetic energy and give rise to a variety of novel quantum states including superconductivity, Mott-like insulating states and orbital magnetism [17,18]. Such moiré heterostructures composed of 2D materials with a relative rotation angle or lattice mismatch have been an important condensed matter system to study the strong correlation physics[19–25]. Combining the interface engineered ferroelectricity and strong correlations in moiré heterostructures provides a great opportunity to create novel quantum states such as ferroelectric superconductivity [26,27].

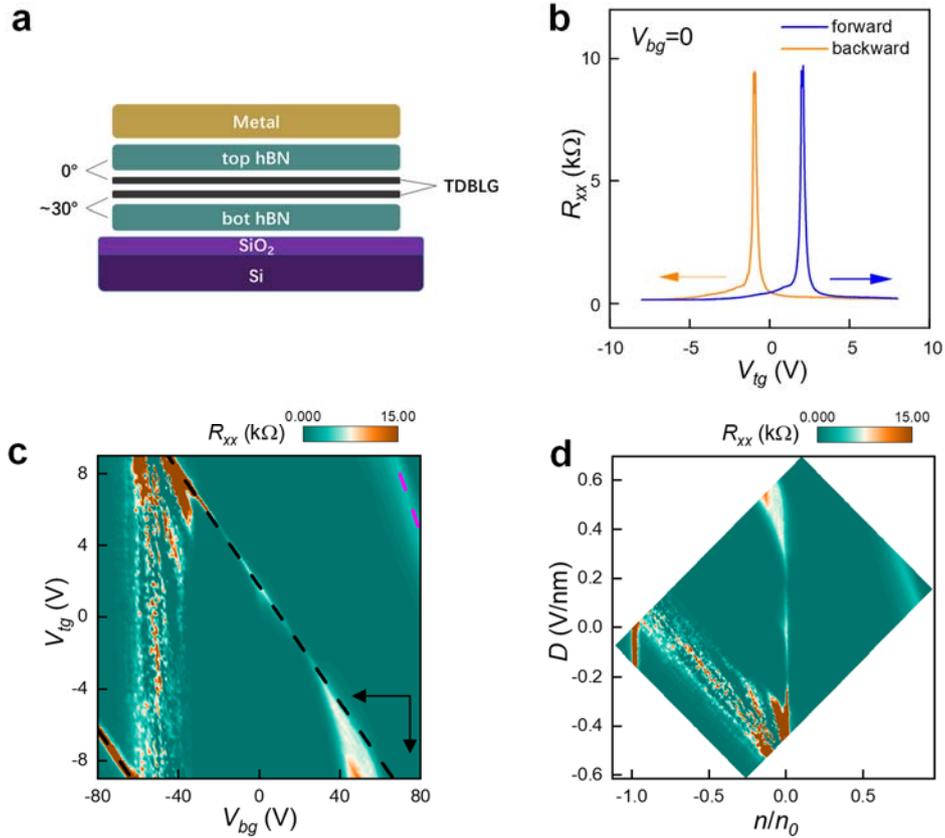


Fig. 1 Transport characteristics of TDBLG device. **a**, Schematic of dual-gate TDBLG device. **b**, Four-terminal longitudinal resistance R_{xx} as a function of top gate voltage V_{tg} , for forward (blue) and backward (orange) scans, respectively, when $V_{bg} = 0$. **c**, Dual-gate mapping of four-terminal longitudinal resistance $R_{xx}(V_{bg}, V_{tg})$ by fast sweeping V_{bg} and changing V_{tg} step by step. The black arrows indicate the sweeping and stepping directions of gate voltages. The black and magenta dash lines highlight the resistance peak ridges. **d**, Converted resistance map as a function of filling factors n/n_0 and displacement field D .

Here in this work, we study the quantum transport of twisted double bilayer graphene (TDBLG), where two bilayer graphene are stacked and rotated by a small angle with respect to each other[19,20,22]. TDBLG is a highly tunable correlated system with rich phase diagram. The correlated states are highly sensitive to twist angle, out-of-plane displacement field and carrier

density, and are demonstrated to be spin-polarized and electrically switchable magnetism. The combination of magnetic states and interface engineered ferroelectricity in TDBLG is promising to realize multiferroicity. The stack was fabricated using standard cut-and-stack transfer method, and TDBLG was encapsulated by two hBN flakes. During the fabrication, TDBLG is intentionally aligned with its top neighbouring hBN, and the top and bottom hBN are rotated by $\approx 30^\circ$. A dual gate configuration was used, allowing to tune charge carrier density n and out-of-plane displacement field D independently. The details of the sample fabrication can be found in Supplementary Materials. Fig. 1a plots the schematic of the final device, and the determination of crystal orientation is shown in Fig. S1. In the following, we will report the observation of asymmetric gating behaviours of top gate voltage V_{tg} and back gate voltage V_{bg} .

Fig. 1b displays the dependence of the four-terminal longitudinal resistance R_{xx} on the top gate voltage V_{tg} when $V_{bg} = 0$. The resistance peak is the location of the charge neutrality point (CNP), where the density of states (DOS) is at minimum. Surprisingly, a huge ferroelectric hysteresis appears between the forward and backward scans. This hysteresis is similar to that observed in bilayer graphene(BLG)/hBN heterostructures[11–13], and it appears in a delayed fashion, that is, the resistance peak appears at positive V_{tg} side for forward scan (blue), and negative V_{tg} side for backward scan (orange).

To further characterize the transport behaviour of our device, we take dual-gate mappings. We first fast-scan V_{bg} and change V_{tg} step by step. Fig. 1c plots four-terminal longitudinal resistance $R_{xx}(V_{bg}, V_{tg})$ mapping for backward scan, exhibiting typical transport features of TDBLG, although the absence of correlated states at fractional fillings. In addition to the main charge neutrality point, two band insulating states appear at both electron and hole sides, resulting from the full fillings of 1st conduction and valence bands. Like previous reports, the increasing out-of-plane displacement field D first closes and then reopens the gap at the main CNP. Usually the resistance peaks in dual-gate mapping run from top left to bottom right with a negative slope $-C_{bg}/C_{tg}$, where C_{bg} and C_{tg} are the capacitance per area of back and top gates, respectively. Therefore, the three resistance peaks should run parallel to each other, as highlighted by the black dash lines in Fig. 1c. However, the slope of the resistance peak ridge at the full filling of 1st conduction band, highlighted by the magenta dash line is two times larger than that at main CNP and the full filling of 1st valence band. This unexpected behaviour is clearly seen when we replot Fig. 1c in terms of charge carrier density n and displacement field D by calculating $n = (C_{bg}V_{bg} + C_{tg}V_{tg})/e$ and $D = (C_{bg}V_{bg} - C_{tg}V_{tg})/2\epsilon_0$ where ϵ_0 is the vacuum permittivity. Here we choose the symmetric point on the main CNP resistance peak ridge as the global CNP. We will discuss the estimations of C_{tg} and C_{bg} later. Fig. 1d shows the $R_{xx}(n/n_0, D)$ and the resistance peaks at main CNP and hole side locate vertically at $n/n_0 = 0$ and -1 as expected, while the resistance peak on the electron side is tilted. If we reverse the scan direction, scanning V_{bg} forward from negative side to positive side as shown in Fig. S2a-b, the band insulating state at the full filling of 1st conduction band behaves normally while the slope of the insulating state at the full filling of 1st valence band is two times larger than expected. Fig. S2c plots the resistance difference between forward and backward scans, and a huge hysteresis loop is clearly seen, suggesting the unconventional transport behaviour in our TDBLG device. We also note that in Fig. S2c, the main CNP resistance peak ridge shifts along V_{tg} axis. In Fig. 1c and Fig. S2a, we take the mappings by stepping V_{tg} from $+9$ V to -9 V. We also measure the data by stepping V_{tg} from -9 to $+9$ V, as shown in Fig. S2d-f, and we find that the stepping direction doesn't influence the transport behaviour. The charge carrier of the full filling of 1st band $n_0 \approx 6.9 \times 10^{12} \text{ cm}^{-2}$, corresponding to the twist angle 1.72° of TDBLG. The twist angle is also confirmed by the Brown-Zak oscillation as shown in Fig. S3.

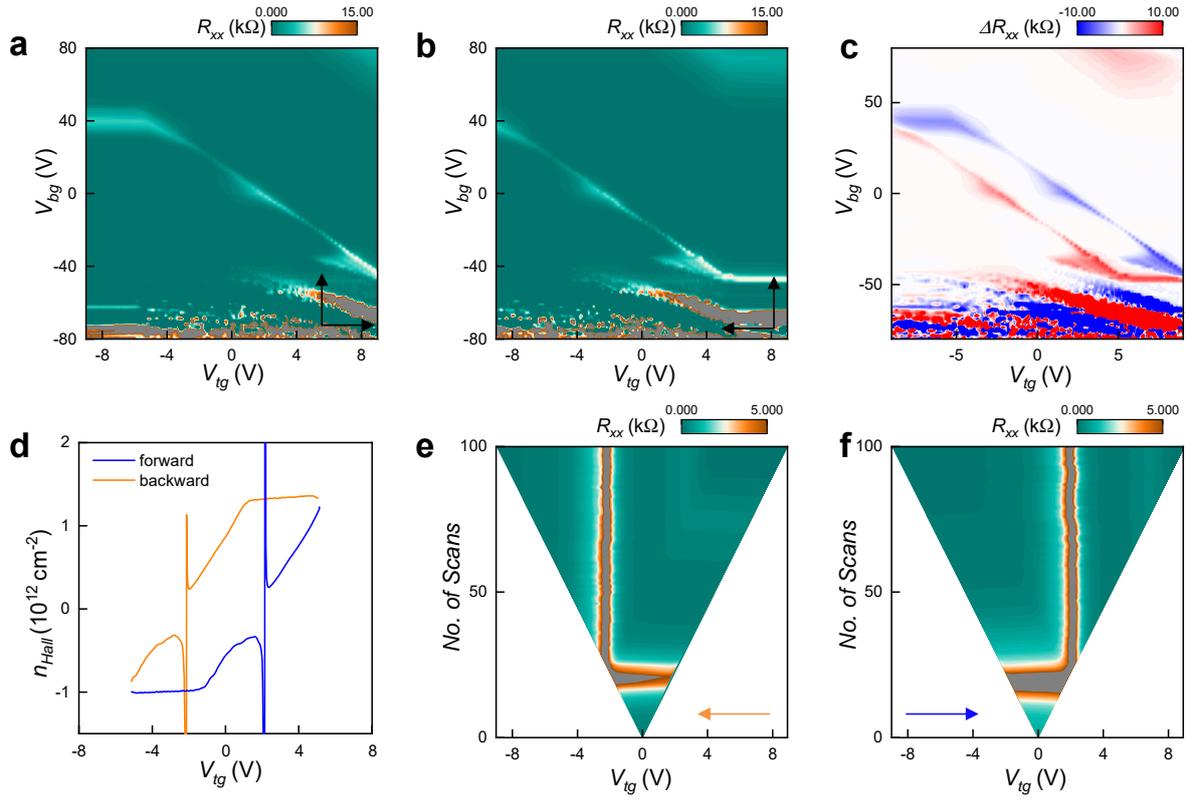


Fig. 2 Layer-specific anomalous screening and hysteretic transport behaviour as a function of top gate voltage. **a-b**, Four-terminal longitudinal resistance mappings $R_{xx}(V_{tg}, V_{bg})$ for forward (**a**) and backward scans (**b**) of V_{tg} . Black arrows indicate the scan directions of gate voltages. **c**, The resistance difference between (**a**) and (**b**). **d**, Carrier density extracted from Hall effect measurement as a function of V_{tg} when $V_{bg} = 0$. **e-f**, Hysteretic transport behaviour by gradually increasing V_{tg} sweep limits for forward (**f**) and backward (**e**) scans.

Based on the data in Fig. 1b and Fig. S2c, we conclude that both top and back gates cause huge hysteresis in our device. However, we will show that these two gates tune the device in different ways. We first focus on the transport behaviour tuned by V_{tg} . Fig. 2a and b plot $R_{xx}(V_{tg}, V_{bg})$ mappings for forward and backward scans of V_{tg} , respectively. Strikingly, we find that the transport behaviour in Fig. 2a-b is very different from that in Fig. 1c and Fig. S2a when we fast-scan V_{bg} . The dual-gate mappings in Fig. 2a and b apparently can be separated into two different regions. In the forward scan mapping (Fig. 2a), the CNP resistance peak ridge runs parallel to V_{tg} axis for the gate voltage from -9V to -5.2V, suggesting the top gate voltage is screened and not working. Above this screening region, the CNP resistance peak ridge behaves normally and depends on both gates. Similarly, a screening region appears in the range 5.2V to 9V in the backward scan (Fig. 2b). Following previous works[11,12], we refer this screening region as layer-specific-anomalous-screening (LSAS). Comparing Fig. 2a and b, we note that LSAS region only appears when we start scanning the top gate. In other words, it appears when we reverse the scan of V_{tg} . In the normal region, the slope of the resistance peak is ~ -6.2 , which is the coupling ratio of back and top gate voltages $-C_{tg}/C_{bg}$. Similar behaviours have been observed in the moiré heterostructures of bilayer graphene aligned with hBN. Fig. 2c displays the resistance difference between Fig. 2a and b. A huge hysteresis loop is clearly seen and the hysteresis shifts along V_{tg} . In Fig. S2c, the hysteresis also shifts along V_{tg} axis, hinting the asymmetric gating of V_{tg} and V_{bg} .

To further investigate the gating of V_{tg} , we measured the Hall effect, R_{xy} for both $B = +1$ T and -1 T, and symmetrize the transverse $R_{xy}(1T) = (R_{xy}(+1T) - R_{xy}(-1T))/2$. The calculated Hall density is shown in Fig. 2d. In the forward scan, the Hall density is almost independent on V_{tg} in the LSAS region, and increases linearly afterwards. This behaviour is reversed in the backward scan, forming a hysteresis loop. By fitting $n_{Hall}(V_{tg})$ in the linear region, we can extract the capacitance of top gate, $C_{tg} \approx 5.3 \times 10^{-4}$ F/m². Moreover, we also observed the similar ratchet effect as reported in Ref[13], shown in Fig. S4a. Ferroelectric hysteresis usually depends on the scan limit and history of external electric field. In Fig. 2e and f, we checked the hysteresis by gradually increasing V_{tg} scan limit from 0 to ± 9 V. When V_{tg} scan range is within -1.9 to $+1.9$ V, the system is trapped in the screening region. This is also confirmed by the dual gate mapping shown in Fig. S4b and c. In this measurement, we limit V_{tg} between -1 and $+1$ V, and step V_{bg} from -80 V to $+80$ V. Surprisingly, the hysteresis disappears and the CNP peak ridges only run parallel to V_{tg} axis. When scan limit is larger than 1.9 V, the hysteresis appears and positions of CNP in forward and backward scans are independent on scan limits.

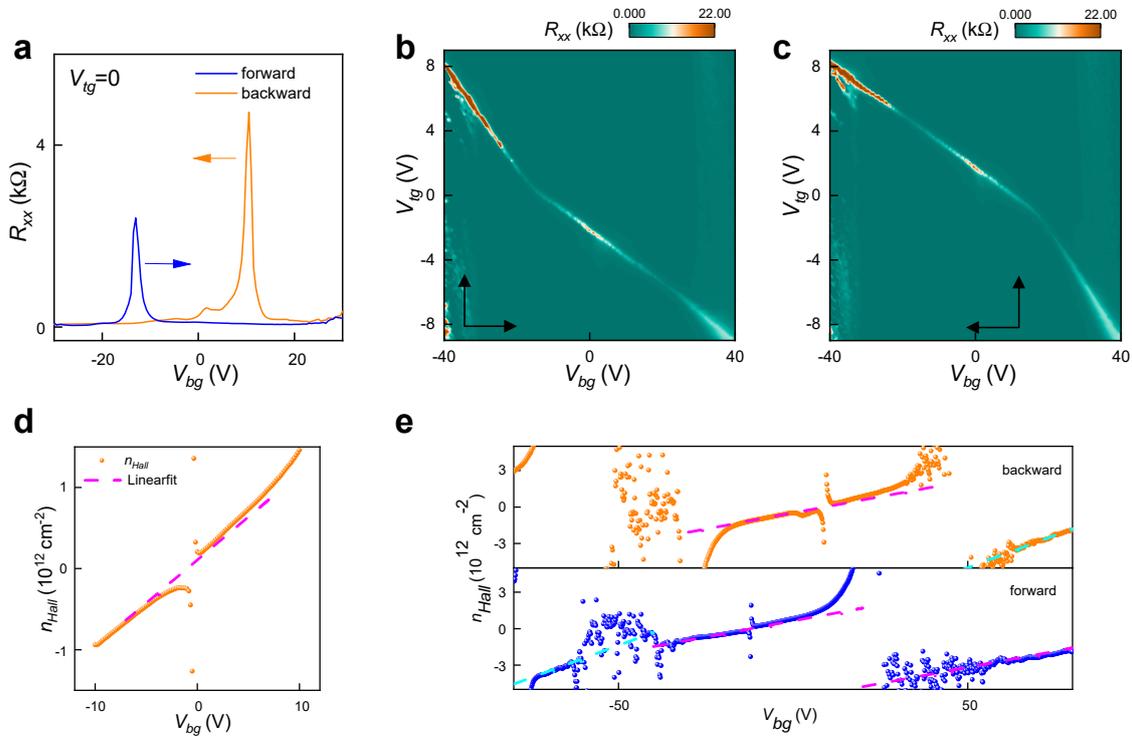


Fig. 3 The anomalous gating and hysteretic transport behaviour as a function of back gate voltage. **a**, Four-terminal longitudinal resistance as a function of back gate voltage V_{bg} , for forward (blue) and backward (orange) scans, respectively when $V_{tg}=0$. **b-c**, Dual-gate mapping of four-terminal longitudinal resistance $R_{xx}(V_{bg}, V_{tg})$ for forward (**b**) and backward (**c**) scans of V_{bg} . The black arrows indicate the sweeping and stepping directions of gate voltages. **d-e**, Hall carrier density as a function of V_{bg} when V_{bg} sweep limit is between $(-10\text{V}, +10\text{V})$, and the system is stuck in the anomalous region (**d**), and $(-80\text{V}, +80\text{V})$ (**e**). Scattered lines are experimental data, and dash lines are linear fittings.

We now turn to investigate the hysteresis as a function of back gate voltage. Fig. 3a plots the dependence of four-terminal longitudinal resistance R_{xx} on back gate voltage V_{bg} , for both forward (blue) and backward (orange) scans when $V_{tg}=0$. Similar to the result as a function of V_{tg} shown Fig.

1b, a huge hysteresis is also present as a function of V_{bg} . On the other hand, however, there are two main different features by comparing Fig. 1b and Fig. 3a. First, the hysteresis in Fig. 3a manifests in an advanced fashion, i.e., the resistance peak appears on negative V_{bg} side for forward scan, and positive side for backward scan, while it is in a delayed fashion in Fig. 1b. Second, the magnitude of the resistance peaks in forward and backward scans are different dramatically. As shown in Fig. 3a, the resistance peak in backward scan is $\approx 4.7 \text{ k}\Omega$, while it is $\approx 2.3 \text{ k}\Omega$ in forward scan. In Fig. 1b, the magnitudes of the CNP resistance peaks are the same. The different resistance peak magnitudes suggest that the out-of-plane displacement field changes dramatically for forward and backward scans. These two different observations of the hysteresis as a function of V_{tg} and V_{bg} indicate that our dual-gate device is gated asymmetrically.

Fig. 3b and c display $R_{xx}(V_{bg}, V_{tg})$ mappings by fast-scanning V_{bg} and stepping V_{tg} . It's the same data as Fig. 1c, but with a smaller V_{bg} scan range between -40V and +40V, making the analysis simpler. Similar to the observations in Fig. 1c, we find that the CNP resistance peaks follow two different slopes. In Fig. 3b of forward scan, the slope for the range of -15.7V to 40V is $\approx -0.16 = -C_{bg} / C_{tg}$, while from $V_{bg} = -40\text{V}$ to -15.7V, the slope is two times larger $\approx -0.32 = -2 * C_{bg} / C_{tg}$. In Fig. 3c of backward scan, the slope for the range of -40V to 15.7V is ~ 0.16 , and it is -0.32 from $V_{bg} = 15.7\text{V}$ to 40V. The region with the slope of $-C_{bg} / C_{tg}$ is normal state, as the change of charge carrier induced by one gate is compensated by the other gate. Furthermore, when we reduce the scan range to even smaller range between -10V and 10V, we find that the system is stuck in the anomalous slope region, as shown in Fig. S5a and 5b. In this mapping, we scan V_{bg} from -10V to 10V, and step-scan V_{tg} from -9V to 9V, the same as in Fig. 3b-c. The slopes of the CNP resistance peaks are both -0.32. Moreover, the hysteresis disappears when the system stuck in the anomalous slope region. The observation is very similar to that of V_{tg} , while V_{tg} is screened in small range. This two-times-larger slope is very bizarre and unexpected, meaning that the effective capacitance of the back gate is two times larger than normal.

To further understand the two regions, we measure the Hall effect as a function of V_{bg} and extract the effective capacitance of back gate. First, we study the Hall effect when V_{bg} scan limit is small, between -10V and 10V, where the system is trapped in the anomalous slope region, and the Hall carrier density for this region is displayed in Fig. 3d. Magenta dash line is the linear fit to n_{Hall} , and the fitting capacitance is $C_{effective} \approx 1.7 \times 10^{-4} \text{ F/m}^2$. In our device, we use heavily doped silicon substrate as back gate, and the dielectric material is 300nm-thick SiO_2 , of which the geometry capacitance per unit area is $C_{geometry} = \epsilon_r \epsilon_0 / d$, where $\epsilon_r = 3.9$ is the dielectric constant of SiO_2 , ϵ_0 the vacuum permittivity and $d = 300\text{nm}$ the thickness of SiO_2 . The estimated back gate geometry capacitance of our sample should be $C_{geometry} \approx 1 \times 10^{-4} \text{ F/m}^2$. Therefore, the extracted $C_{effective}$ is much larger than expected, not to mention that the bottom hBN is on the order of tens of nanometers, and the geometry capacitance should be further reduced. We then increase the scan range of V_{bg} to $\pm 80\text{V}$ and repeat the Hall measurement. The results are shown in Fig. 3e for forward and backward scan, respectively. In both scans, the CNP resistance peaks are in the normal TDBG transport behaviour region, and the extracted back gate capacitance $C_{bg} \approx 0.85 \times 10^{-4} \text{ F/m}^2$, as denoted by the magenta dash lines. On the other hand, in the anomalous region, the effective back gate capacitance is two times larger, and estimated as $\approx 1.7 \times 10^{-4} \text{ F/m}^2$, shown by the cyan dash lines, same with Fig. 3d.

With this observation of unexpected larger effective back gate capacitance, we are able to explain the aforementioned two unexpected features in Fig. 3a. First, for an undoped graphene system, the CNP resistance peak should locate at zero gate voltage. But if the effective capacitance is

doubled when we start scanning and then goes back to normal, the graphene will behave like it is n -doped (p -doped) for forward (backward) scan when $V_{bg} = 0$, that is, the CNP resistance moves to negative (positive) gate voltage in forward (backward) scan. Second, although the effective capacitance doubles, only half of the charges are injected from ground to the bottom graphene layer by back gate, and the other half should originate from some other mechanism. Considering that the resistance peak magnitude varies dramatically between forward and backward scans, we speculate that the other half of charges are injected to the top graphene layer, causing a finite displacement field vertically. Therefore, electrons are injected to top graphene layer in the forward scan, and removed from the top graphene layer in the backward scan. In this case, the effective back gate capacitance is doubled, but D are different for forward and back scans, giving rise to different band gaps and resistance peak magnitudes. So far, we have established the fact that the top gate is anomalously screened, while the back gate is anomalously doubly efficient in our device.

Based on the observations of the asymmetric gating in our sample, i.e., the top gate is anomalously screened, while back gate is anomalously doubly effective in injecting charges into graphene, it seems there exists an electric polarization between top hBN and graphene, which produces an out-of-plane displacement field D_p that can be tuned by external D_{ext} (Fig. 4a). Therefore, the total charge carrier in graphene is $n_{tot} = n_t + n_p + n_b = \frac{2\epsilon_0}{e}(-D_t - D_p + D_b)$, where n_t, n_p, n_b are charges induced by top gate displacement field D_t , the polarization displacement field D_p and back gate displacement field D_b , respectively. Note that since the electric polarization is above graphene, n_p accumulates on top graphene layer. If we assume the change of D_p is negatively proportional to D_{ext} , $\Delta D_p = -\Delta D_{ext}$, and D_p saturates at $\pm D_{saturation}$ (Fig. 4b), we are able to explain the gating behaviour of both top and back gates. When we scan V_{tg} , $\Delta D_p = -\Delta D_t$, so the change of total carrier density $\Delta n_{total} = 0$. In this case, V_{tg} is screened. When D_p is saturated, n_{tot} is only tuned by top gate and the system goes into normal region. When we scan V_{bg} , $\Delta D_p = -\Delta D_b$, so $\Delta n_p = \Delta n_b$ and $\Delta n_{tot} = 2\Delta n_b$. In this case, V_{bg} is doubly effective in injecting electrons or holes into graphene. However, Δn_p accumulates on the top graphene layer, and Δn_b accumulates on the bottom graphene layer. Therefore, the total displacement field is different for forward and backward scans of V_{bg} . When D_p is saturated, n_{tot} is only tuned by back gate and the system goes into normal region.

Thanks to the dual-gate configuration of our sample, we can tune the external carrier density n_{ext} and external displacement field D_{ext} independently. When we fix D_{ext} and scan n_{ext} , the hysteretic behaviour should be absent as the D_p is fixed. Indeed, that's exactly what we observed experimentally. Fig. 4c displays R_{xx} as a function n_{ext} under $D_{ext} = 0.1$ V/nm (white dash line in Fig. 4d). The hysteresis between forward (blue) and backward (orange) scans is absent as expected. However, we note that the CNP peak is located at positive n_{ext} side, suggesting the graphene is p -doped. The full mapping $R_{xx}(n_{ext}, D_{ext})$ is shown in Fig. 4d. In this measurement, we scan n_{ext} from negative to positive, and step D_{ext} from positive to negative, as indicated by the black arrows. Fig. 4e shows the same measurement, but we step D_{ext} from negative to positive side. This time, the CNP peak moves to negative n_{ext} , suggesting graphene is n -doped. The different doping between Fig. 4d and e can also be explained by the simple electric polarization model. When we change D_{ext} step by step from positive to negative value, D_p increases correspondingly, and finally D_p saturates at $+D_{saturation}$, which dopes graphene by injecting holes to the top graphene layer. Similarly, when we increase D_{ext} , D_p decreases and finally D_p saturates at $-D_{saturation}$, doping graphene by injecting electrons to the top graphene layer. Finally, when we fix n_{ext} and scan D_{ext} , shown in Fig. 4f, D_p changes in correspondence with D_{ext} . As a result, we are changing graphene carrier density by tuning D_p . See Fig. S7 for more data of similar n_{ext} scans.

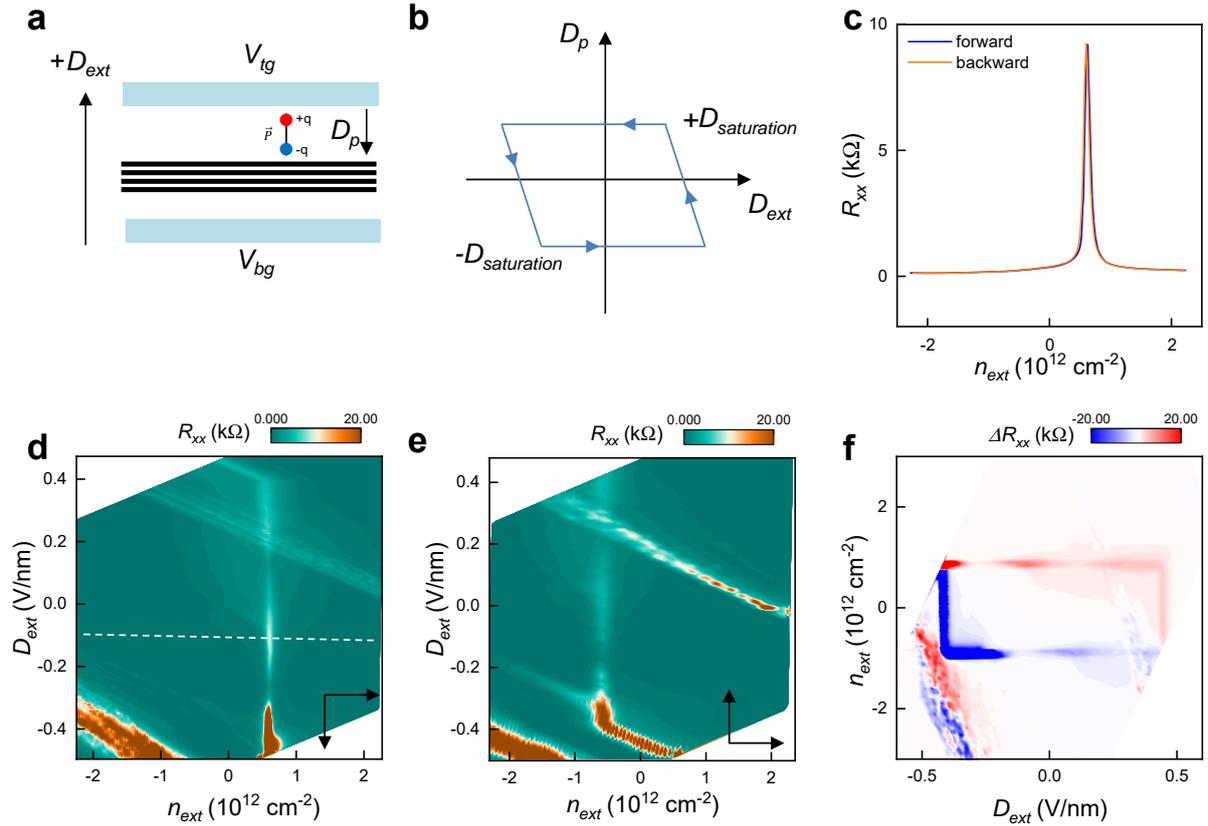


Fig. 4 A simple electrostatic model and the transport dependence on external carrier density and out-of-plane displacement field. **a**, Schematic of an electrostatic model. The arrow pointing upward indicates the positive direction of D_{ext} . A spontaneous electric polarization D_p is located between graphene and top hBN. **b**, The dependence of the polarization displacement field D_p on external D_{ext} . $D_{saturation}$ is the saturation value of D_p . **c**, Four-terminal longitudinal resistance as a function of external carrier density n_{ext} , for forward (blue) and backward (orange) scans, respectively when $D_{ext}=0$. **d-e**, Mappings of four-terminal longitudinal resistance R_{xx} (n_{ext} , D_{ext}) for forward (**e**) and backward (**d**) scans of n_{ext} . The black arrows indicate the sweeping and stepping directions of n_{ext} and D_{ext} . **f**, The resistance difference between forward and backward scans of D_{ext} . The raw data is shown in Fig. S6.

So far, the role that the moiré pattern between two BLG in TDBLG plays is unclear. AB-BA stacked TDBLG has been predicted to host ferroelectricity due to interlayer sliding[28,29]. However, this case doesn't apply to our AB-AB stacked sample. The hysteretic transport behaviour in this work is more likely to result from the moiré alignment between graphene and hBN. To check if the aforementioned electric polarization model applies to other graphene systems, we fabricated a monolayer graphene stack aligned with both top and bottom hBN flakes. The optical image of the sample is shown in Fig. S8a. We made two Hall bars, named as M1 and M2, from the same graphene stack. Strikingly, we find that M1 and M2 behave differently although they share the same device structure. As shown in Fig. S8b and c, the device M1 exhibits normal transport behaviour, and the CNP resistance peak ridge runs from top left to bottom right in dual-gate mappings without any hysteresis. On the contrary, however, M2 shows similar LSAS as a function of V_{tg} , as displayed in Fig. S8d-f. V_{tg} is anomalously screened when we reverse the scan direction, and graphene behaves normally afterwards. The hysteresis loops are clearly seen in the resistance difference between forward and backward scans, shown in Fig. S8f. Fig. S9 plots additional transport data of device M2.

When we only scan positive V_{tg} , the hysteresis loop reduces (Fig. S9a-b), and the system is trapped in the screening region when we scan V_{tg} within a small range from -2.5 to +2.5V (Fig. S9c). This behaviour is very similar to TDBLG shown in Fig. S4b-c. However, when we fast-scan V_{bg} , the transport properties of M2 are dramatically different from that of TDBLG. No hysteresis is observed as a function of V_{bg} . Instead, three distinct regions where the resistance peaks follow different slopes appear in Fig. S9d. Two regions are normal and share the same slope, while the resistance ridge in the middle one runs parallel to V_{tg} axis. This phase diagram shown in Fig. S9d is very similar to that observed in BLG/hBN moiré heterostructures, as reported in Ref[11–13], where V_{bg} is named as control gate that controls the hysteresis.

We now provide a brief discussion on the underlying mechanism of the ferroelectric hysteresis. So far, most the hysteresis reported in graphene devices are from the aligned samples, including BLG[11–13], TDBLG and MLG in this work. It's reasonable to conclude that the alignment between graphene and hBN plays a critical role in such devices. However, our results in MLG devices suggest that the alignment is a necessary but not a sufficient condition to realize such ferroelectric behaviour in graphene systems. This could explain the absence of hysteresis in other aligned BLG works[30,31], suggesting that more ingredients are needed to achieve the ferroelectricity in graphene moiré heterostructures. Since MLG devices M1 and M2 are fabricated from the same stack and share the same device structure, the first origin we consider is the local trapping defects or charge injections in hBN dielectrics. Such extrinsic factors are very unlikely since most of the ferroelectricity are observed in aligned samples. Moreover, the ferroelectricity resulting from trapping states usually has a strong dependence on sweeping rate, which is not the case in our work as well as previous reports[12]. Another difference between M1 and M2 is the local twist angle and strain variations. Marginally twisted bilayers usually undergo lattice reconstructions, which lead into preferential stacking domains and highly strained domain wall networks[32]. It has been predicted that the nodes of such domain wall networks possess the largest strains. Such strains in moiré superlattices could cause self-organized quantum dots[32] or pseudo-magnetic field induced Landau levels in graphene[33,34], resulting into electron/hole localization on the moiré length scale. Such localised states could be responsible for the electric polarization in Fig. 4a-b. We note that such lattice reconstructions strongly depend on temperatures and thermodynamic process. Indeed, it is reported that the magnitude of hysteresis in BLG/hBN heterostructures varies within different thermal cyclings[11], which could serve as an experimental evidence of localized states resulting from local strains.

Although the simple electric polarization model could be used to explain the LSAS in M2, the reason of the the absence of hysteresis as a function of V_{bg} in M2 is unclear. The discrepancies between TDBLG device and M2 are the thickness, and the additional moiré pattern between two BLG. Different graphene thickness will cause different screening and charge distribution within the layers. Graphene samples with other layers are needed to systematically study the effect of thickness, and control devices of tetralayer graphene[35] could be used to investigate the effect of additional moiré pattern between two graphene layers. Nevertheless, more theoretical and experimental works are required to to tackle the problem of mysterious ferroelectricity in graphene/hBN moiré heterostructures.

Data availability

All relevant data are available from the corresponding author on reasonable request.

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Author contributions

Y.S. conceived the presented idea and directed the project. Y.S., L.C., H.L. and Z.W. performed transport measurements. Y.S., L.C., H.W., R.M., Z.S. and M.F. fabricated devices. Y.S., L.C. and H.L. performed data analysis. Y.S. and L.C. contributed to the interpretation of data. K.W. and T.T. grew hBN single crystals. Y.S. and L.C. contributed to the writing of the manuscript. All authors discussed the results and commented on the manuscript.

Competing interests

The authors declare no competing interests.

Supplementary Materials

S1. Sample fabrication and electrical transport measurement

The graphene and hBN nanosheets are mechanically exfoliated on a 285nm thick SiO₂/Si substrate, and the layer numbers is determined by optical microscope contrast and Raman spectroscopy. We use the stamp consisting of glass slide, PDMS dome, PPC film (15%) to assemble the heterostructure using the dry transfer technique. The stamp is employed to pick up the bottom hBN layer, and the graphene layer and hBN flakes can be picked up through van der Waals (vdW) force. For TDBLG, we cut the BLG using a tungsten tip. The alignment between graphene and hBN is achieved by aligning the sharp straight edges. The final stack is placed on a 285nm thick SiO₂/Si substrate, followed by dissolving PPC film in chloroform and annealing to remove the polymer residue. We follow the standard nanofabrication process to make devices from the stack. We define the electrodes with e-beam lithography and develop with chilled DI water/IPA (1:3), followed by the deposition of metal (5nm Cr and 50nm Au). We use the same process to define the top gate, and etch the samples into Hall bar using RIE or ICP. The doped Si substrate or a graphite film serves as back gate.

Resistance measurements were carried out using standard low-frequency lock-technique with excitation current of few nA range in a commercial cryostat equipped with superconducting magnet. All measurements were taken at the temperature of 1.5K unless specified otherwise. Gate voltages were applied by commercial DC voltage source meter units. Due to contact issues, only two-terminal resistance (R_{2t}) were taken in MLG devices M1 and M2.

S2. Determination of crystal orientation of hBN

The second harmonic generation (SHG) technique was used to characterize the crystal orientation of hBN. In SHG measurements, a Ti:Sapphire femtosecond pulsed laser operating at a wavelength of 800 nm serves as the incident light with excitation power of a few milliwatts. The linearly polarized incident laser beam passes through a sequence of optical elements—half-wave plate, polarizer, analyzer, and another half-wave plate—before reaching the surface of hBN. As the polarization rotates over 2θ when the half-wave plate changes θ , a 180° rotation is sufficient to capture the full dataset. The SHG signal is minimized when the polarization of incident light is along the zigzag direction, and maximized along the armchair direction. When plotting the SHG signal intensity against the polarization direction in a polar coordinate system, a sixfold polarized pattern with a period of 60° is anticipated. Fitting the pattern using $I_{SHG} \propto \cos^2(\theta_{pol} - \varphi)$, where the parameter φ denotes the crystal orientation of hBN.

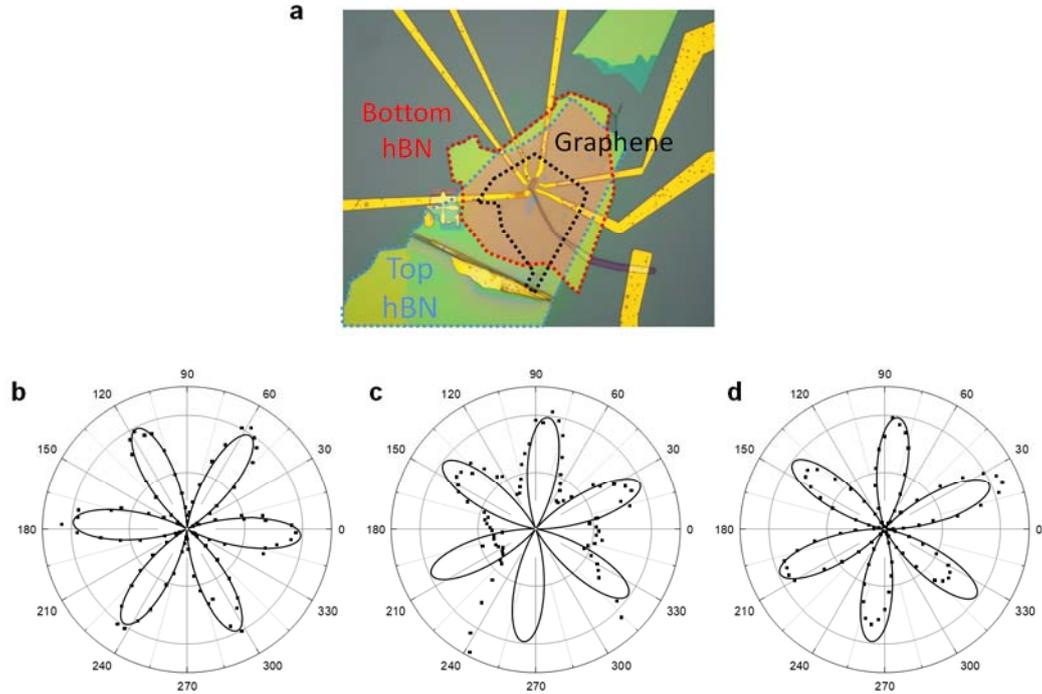


Fig. S1 Alignment of TDBLG. **a**, Optical image of the encapsulated stack of TDBLG. Top hBN, TDBLG and bottom hBN are outlined by blue, black and red dot lines, respectively. **b-d**, Second harmonic generation measurement of top hBN, the etched bottom hBN and a hBN flake, which locates near the bottom hBN and shares the same crystal orientation. The relative rotation angle between top and bottom hBN is $\approx 27^\circ$.

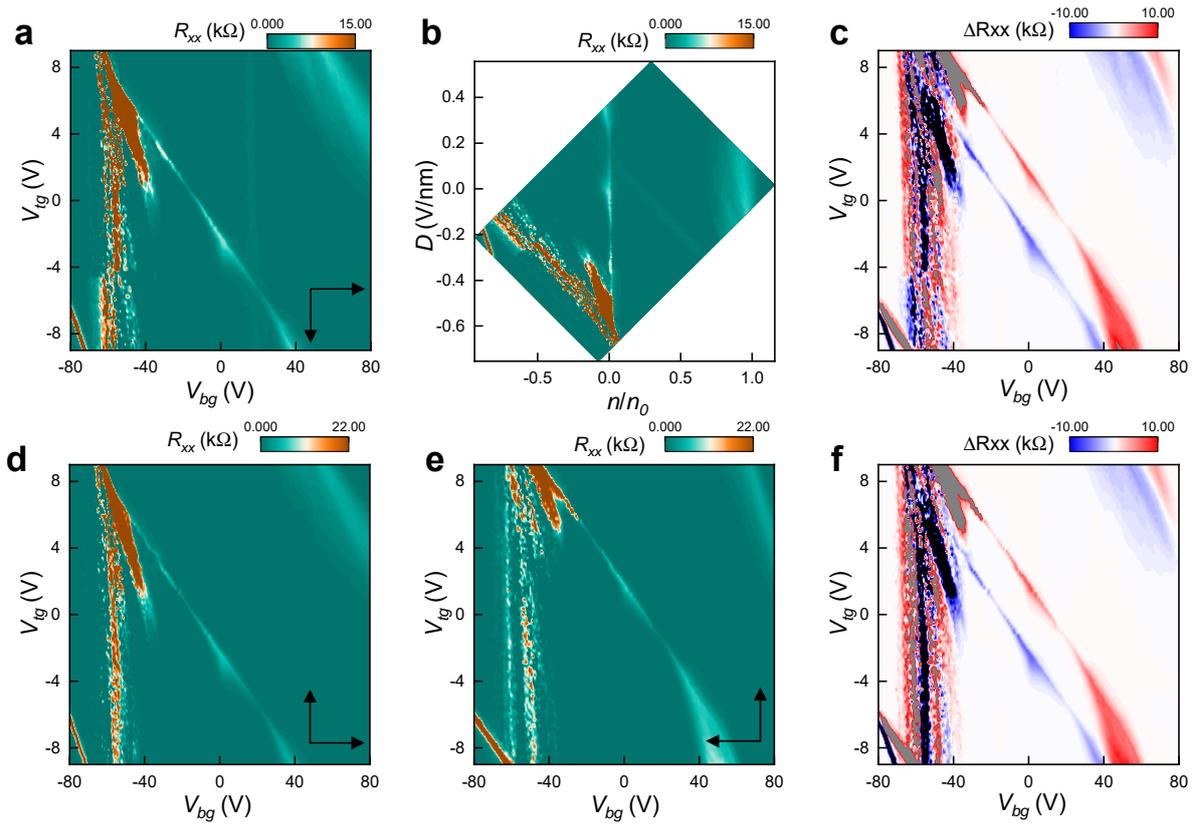


Fig. S2 Transport behaviour by fast-sweeping V_{bg} . **a**, Same data as Fig. 1c for forward scan of V_{bg} . **b**, Converted R_{xx} (n/n_0 , D) from (a). **c**, Resistance difference between Fig. 1c and (a). **d-e**, Longitudinal resistance mappings for stepping V_{tg} from negative to positive value. **f**, the resistance difference between (d) and (e). Black arrows indicate the scanning directions.

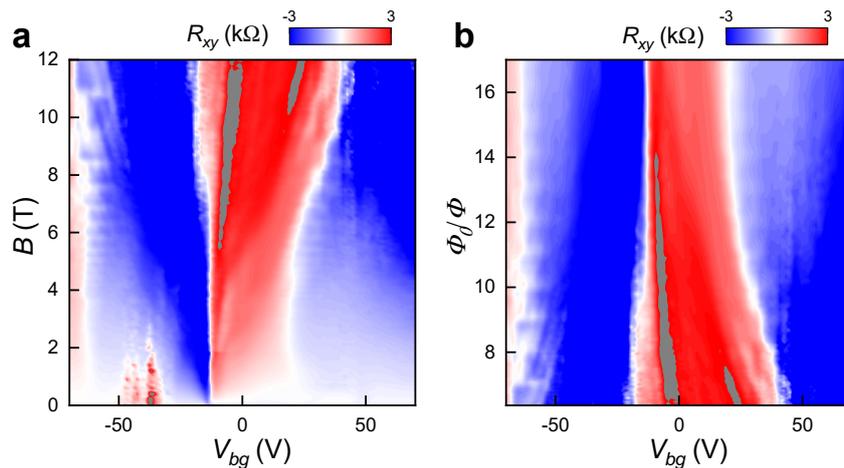


Fig. S3 Transport behaviour in perpendicular magnetic field. **a**, $R_{xy}(V_{bg}, B)$ mapping for backward scan of V_{bg} when $V_{bg} = 0$. **b**, Converted $R_{xy}(\Phi_0/\Phi, B)$ from **a**, where $\Phi_0 = h/e$, h is the Planck constant, e is the electron charge, and $\Phi = BS$ is the magnetic flux through a moiré unit cell.

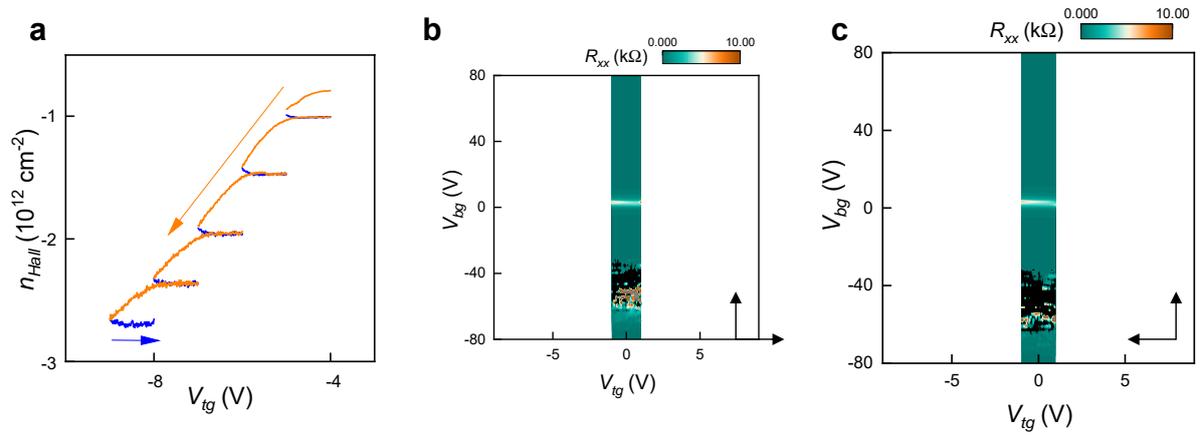


Fig. S4 Anomalous screening of V_{tg} . **a**, Ratchet effect on the hole side as a function of V_{tg} , $V_{bg}=0$. Orange and blue lines are backward and forward V_{tg} scans, respectively. **b-c**, $R_{xx}(V_{tg}, V_{bg})$ dual gate mappings when V_{tg} scan limit is between (-2V, 2V) for forward (**d**) and backward (**c**) scans.

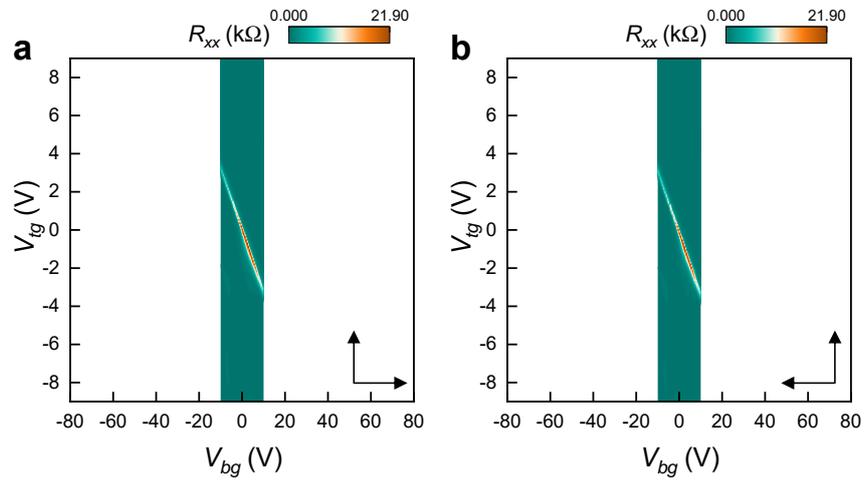


Fig. S5 Anomalous gating of V_{bg} . **a-b**, $R_{xx}(V_{bg}, V_{tg})$ dual gate mappings when V_{bg} scan limit is between (-10V, 10V) for forward (**a**) and backward (**b**) scans.

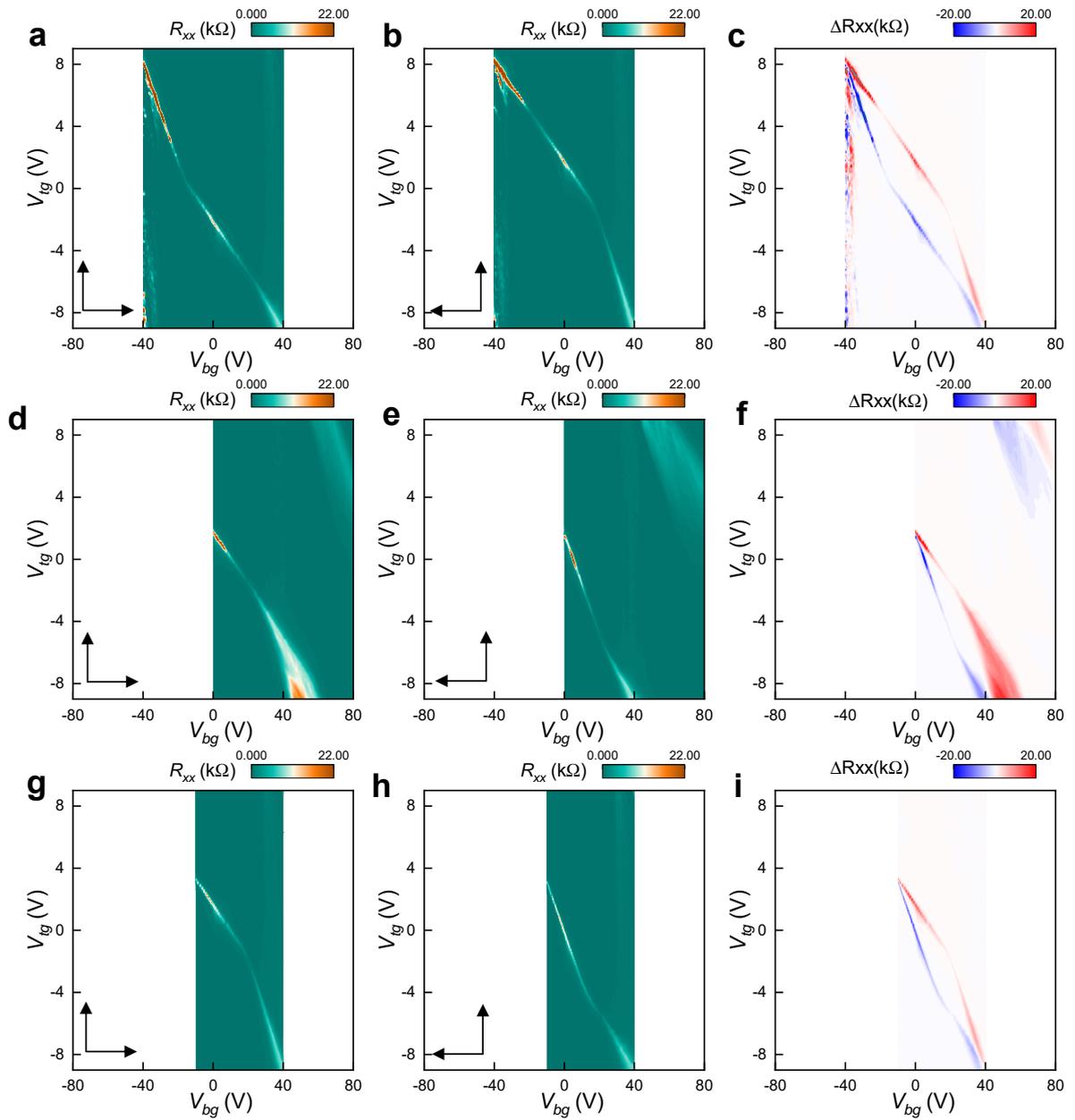


Fig. S6 Additional data on the anomalous gating of V_{bg} . a-b, $R_{xx}(V_{bg}, V_{tg})$ dual gate mappings when V_{bg} scan limit is within -40 to 40V (a-c), within 0 to 80V (d-f) and within -10 to 40V (g-i).

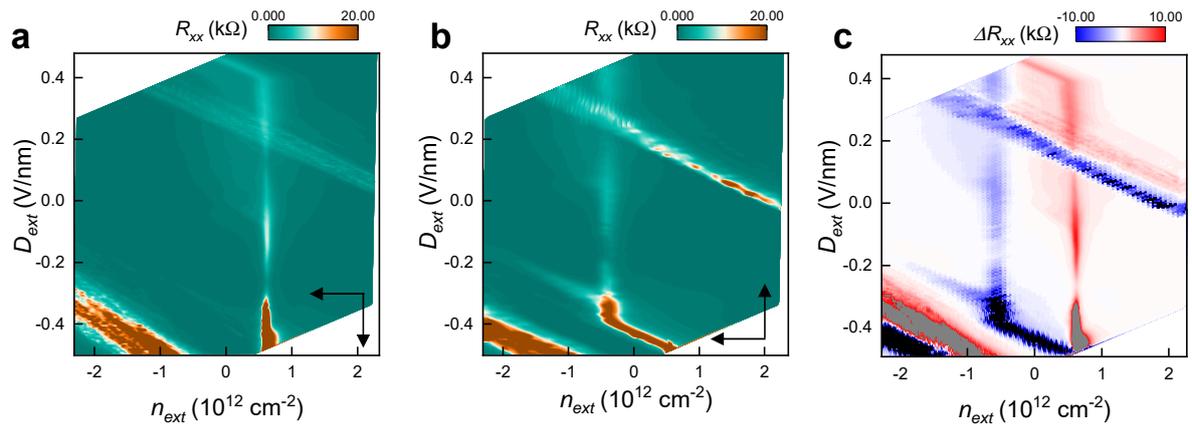


Fig. S7 Additional data on the transport behaviour when fast-scanning n_{ext} . **a-b**, Same data as Fig. 4d-e, but with different scanning directions. **c**, Resistance difference between **a** and **b**.

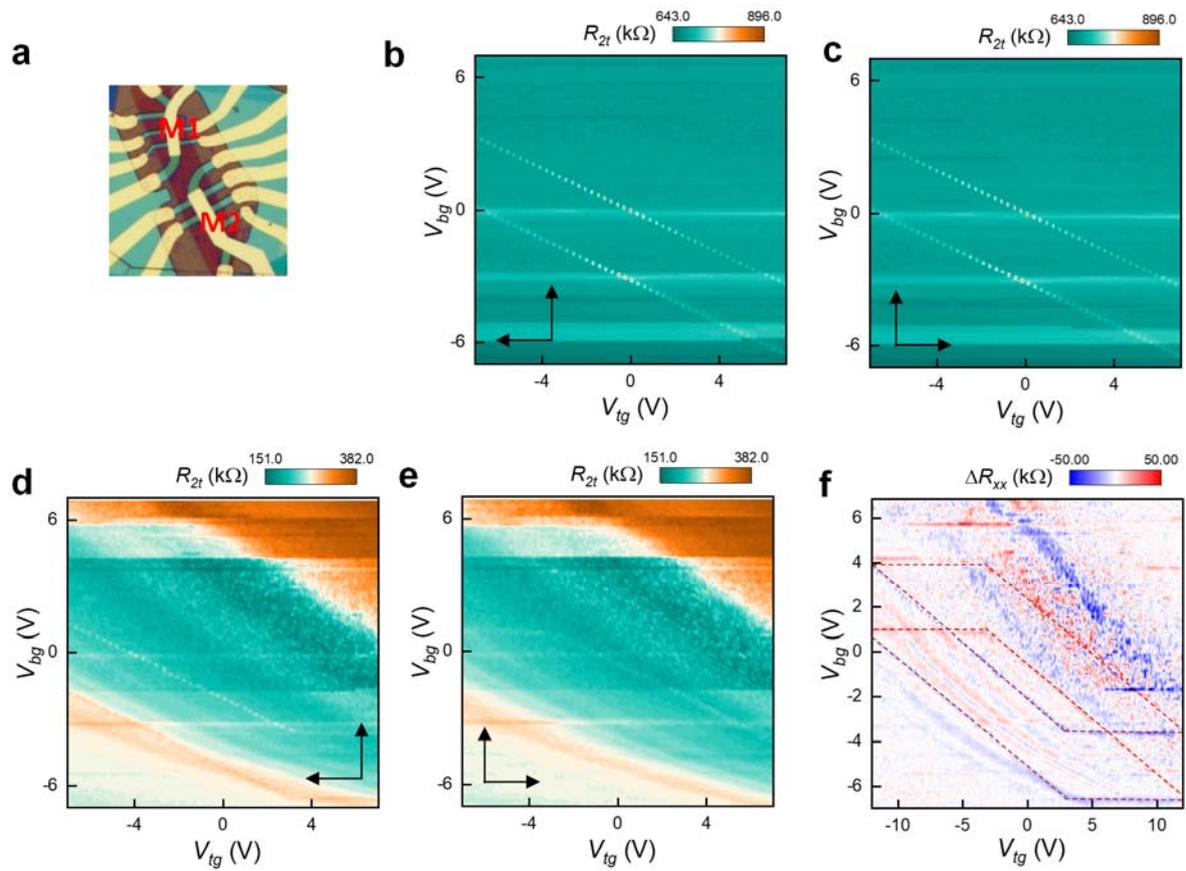


Fig. S8 Distinct transport behaviours of two MLG devices fabricated from the same heterostructure stack. **a**, Optical image of devices M1 and M2. **b-c**, Two-terminal resistance map $R_{2t}(V_{tg}, V_{bg})$ of M1 for backward (**b**) and forward (**c**) scans of V_{tg} . Arrows indicate the scanning directions of gate voltages. **d-e**, Two-terminal resistance map $R_{2t}(V_{tg}, V_{bg})$ of M2 for backward (**d**) and forward (**e**) scans of V_{tg} . **f**, Resistance difference between **d** and **e**. Red dash lines highlight the hysteresis loops.

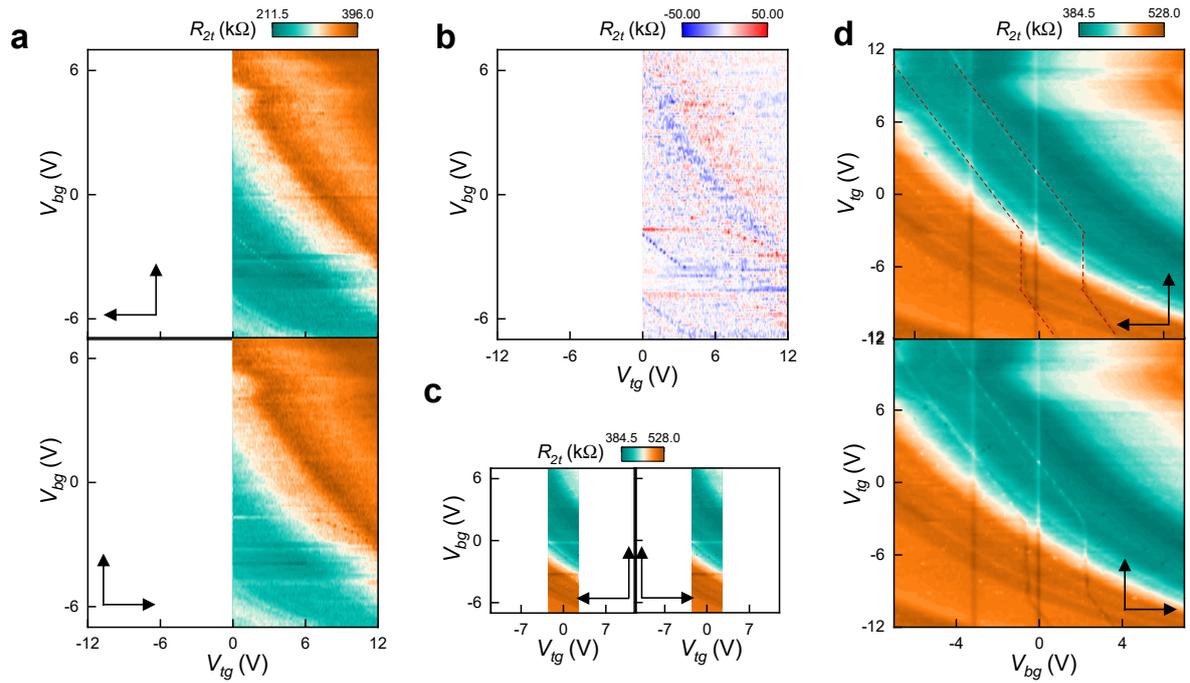


Fig. S9 More data on the transport properties of device M2. **a**, Two-terminal resistance map $R_{2t}(V_{tg}, V_{bg})$ of M2 for backward (top) and forward (bottom) scans of positive V_{tg} . Arrows indicate the scanning directions of gate voltages. **b**, Resistance difference between two maps in **a**. **c**, Same measurement with **a**, but within V_{tg} scan limit from -2 to 2V. **d**, Two-terminal resistance map $R_{2t}(V_{bg}, V_{tg})$ of M2 for backward (top) and forward (bottom) scans of back gate voltage V_{bg} . Red dash lines highlight the two resistance peak ridges.