

# A multi-module silicon-on-insulator chip assembly containing quantum dots and cryogenic radio-frequency readout electronics

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**Abstract**—Quantum processing units will be modules of larger information processing systems containing also digital and analog electronics modules. Silicon-based quantum computing offers the enticing opportunity to manufacture all the modules using the same technology platform. Here, we present a cryogenic multi-module assembly for multiplexed readout of silicon quantum devices where all modules have been fabricated using the same fully-depleted silicon-on-insulator (FDSOI) CMOS process. The assembly is constituted by three chiplets: (i) a low-noise amplifier (LNA), (ii) a single-pole eight-throw switch (SP8T), and (iii) a silicon quantum dot (QD) array. We characterise each module individually and show (i) a gain over 35 dB, a bandwidth of 118 MHz, a minimum noise temperature of 4.2 K, (ii) an insertion loss smaller than 1.1 dB, a noise temperature smaller than 1.1 K across 0-2 GHz, and (iii) single-electron box (SEB) charge sensors. Finally, we combine all elements into a single demonstration showing time-domain radio-frequency multiplexing of two SEBs paving the way to an all-silicon quantum computing system.

**Index Terms**—Cryo-CMOS, cryogenic, fully-depleted silicon-on-insulator (FDSOI), low-noise amplifiers (LNA), quantum computing, reflectometry, single-electron devices, single-pole eight-throw switch (SP8T), spin qubits, time-division multiplexing.

## INTRODUCTION

Quantum computing hardware based on spins in silicon QDs is a promising approach towards a scalable quantum computing system. Particularly, silicon spin qubits have been operated and read out with a precision above the threshold to perform quantum error correction [1]. In terms of scaling, quantum processing units of up to 6 qubits have been fabricated using experimental processes [2] but substantial further scaling may be subject to exploiting silicon’s CMOS manufacturing infrastructure [3] enabling integration with classical cryo-electronics to form a compact quantum computing system [4]. To this purpose, demonstrating QD devices as well as cryo-electronics modules in a industry standard process is a key step towards a fully-fledged quantum processor. Here, we demonstrate a multi-module assembly containing two cryo-electronic modules – a LNA and a Switch – as well as a quantum module – an array of QD sensing devices – all manufactured using GlobalFoundries 22FDX technology. We combine all modules into a time-domain multiple access radio-frequency multiplexing demonstration of SEB charge detectors showing key developmental steps towards an all silicon quantum processing system.

## CRYOGENIC LOW-NOISE AMPLIFIER

To provide cryogenic amplification, we designed a two stage RF LNA IC. Each stage uses a cascoded topology with a passive resonator as load. The internal bias unit and external positive supply of each stage are independent to ensure stability. The first stage uses inductive source degeneration to provide narrow-band input matching. Both stages use thin oxide flipped-well NMOS devices which have shown excellent RF performance in the deep-cryogenic regime [5]. Figure 1(a) shows the simplified schematic of the LNA IC with additional external passives for input and output matching. We integrated the IC and passives in a PCB module (Fig. 3(a) and (b)), and characterized it at 4 K. Figure 1(b) shows the measurement results. We show a peak  $S_{21}$  greater than 35 dB and a 3dB bandwidth of 118 MHz (from 709 MHz to 827 MHz), an input-referred average NT of 6.2 K over the LNA bandwidth, and a minimum NT of 4.2 K at 650 MHz, see Fig. 1(b). Note that the noise match happens below the LNA bandwidth due to changes in the electrical characteristics of the devices in the deep-cryogenic regime compared to the PDK modelled temperature regime. The standby power consumption of the LNA module is 36 mW.

## CRYOGENIC SP8T SWITCH

To provide cryogenic time-domain multiplexing, we designed a SP8T RF switch IC. The IC is comprised of a digital communication and logic block and an analog switch block. The digital block provides external communication using the SPI protocol and the internal control signals to the analog block. The analog block contains eighth switching elements in a series-only topology. The switching elements are thick oxide flipped-well NMOS devices operated in dynamic threshold-voltage mode. Figure 1(c) shows the block diagram of the IC including a simplified schematic of the analog block. We integrated the chip in a PCB module (Fig. 3(c) and (d)), and characterised it at 4K and for the 0-2 GHz input frequency range. Figure 1(d) shows the measurement results. We show an insertion loss of less than 1.1 dB for all channels, a cross-channel isolation better than 35 dB and a NT smaller than 1.1 K. The standby power consumption of the Switch module is less than 100 nW.

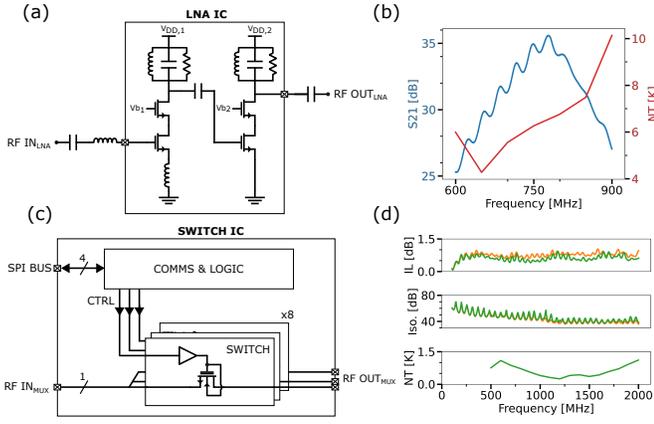


Fig. 1. LNA and Switch ICs (a) LNA circuit schematic. (b) LNA gain (blue) and Noise Figure (red). (c) Switch schematic. (d) Insertion Loss (top), Cross-channel isolation (middle) and Noise Temperature (bottom) vs frequency. Green (orange) trace typical (worst) case. Only typical case shown for Noise Temperature due to measurement uncertainty. Measurements performed at 4 K.

### SINGLE-ELECTRON BOX CHARGE SENSOR

We present results on SEBs charge detectors, ( $SEB_i$  for  $i = 0, 1$ ). The devices are implemented in a narrow channel multi-gate transistor, see Fig. 2(a). When a positive potential, near the threshold voltage, is applied to a gate ( $G_i$ ) placed next to an ohmic contact ( $RX_i$ ), a QD tunnel-coupled to an electron reservoir forms, i.e a SEB. We probe the impedance of the device using RF transmission techniques by applying an RF excitation to  $G_i$  and collecting the transmitted signal on the  $RX_i$  port where a L-shape high-pass matching resonant network of center frequency  $f_i$  is placed. We refer to these matching networks as MN: $i$ , see Fig. 2(b). When electrons cyclically tunnel between the QD and the reservoir due to the RF excitation, a change in the transmission through the device occurs, see Fig. 2(c). Such sharp change in transmission can be used for sensitive charge detection of nearby QDs or qubits [6]. We integrated the chip in a PCB module (Fig. 3(f) and (e)), and perform the measurement on two SEBs, see orange and green traces in Fig. 2(b).

### MULTI-MODULE CRYOGENIC ASSEMBLY

Next, we move on to the cryogenic characterisation of the full assembly. In Fig. 4(a), we show the cryogenic setup. We send an attenuated RF signal to the switch module which acts as a multiplexer (MUX) placed at mixing chamber of a dilution refrigerator with base temperature of 20 mK. The MUX distributes the signal on-demand through channels MUX:0 and MUX:1 to the SEB chiplet also placed at the mixing chamber plate. Then the transmitted signal through each SEBs is impedance-matched at the output using the  $LC$  networks. The signal is then amplified by the LNA and base-band IQ demodulated at room temperature.

We now characterise the S-parameters of the assembly, see Fig. 4(b). First, in blue, we plot a  $S_{21}$  measurement, equivalent to a RF reflectometry test, showing two sharp

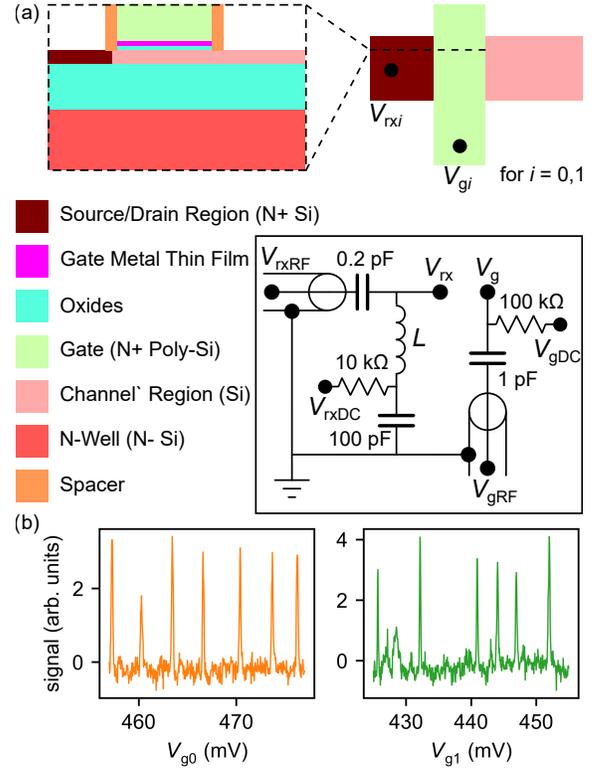


Fig. 2. Single-electron box chiplet. (a) Schematic cross section of the device along the silicon channel direction (top left) and top view (top right). A QD forms in the silicon directly under the gate electrode and is tunnel coupled to the ohmic contact.  $V_{rx_i}$  refers to the ohmic contact potential and  $V_{g_i}$  to the gate potential. We label the different colors in the bottom left and describe the matching network as well as the components in the bias lines in the bottom right of the panel.  $V_{rx(g)DC}$  refer to quasi-static voltages and  $V_{rx(g)RF}$  to radio-frequency voltages. (b) Demodulated response as a function of gate voltage showing charge oscillations for SEB:0,1; orange and green traces, respectively.

resonances at the frequency of the  $LC$  resonators (red dashed lines) from which we determine  $f_i$ . We now characterise the transmission through the assembly,  $S_{31}$ , including the MUX. In orange(green), we activate MUX:0(1) and show the transmission primarily happens through MN:0(1) with an isolation to MN:1(0) of  $> 13$  dB. Additionally, we show measurements when MUX:2,3,7 are active (red, purple and brown lines) indicating a  $> 39$  dB internal MUX isolation. Cross-coupling at the SEB chiplet contributes to the difference in isolation. Finally, in Fig. 4(c), we combine the three modules into a demonstration of multi-frequency time-division multiplexing. We continuously send two RF tones at  $f_i$ . First, for  $t < 400$  ms, we select MUX:0 and detect the charge oscillations as a function of gate voltage in  $SEB_0$  (see the blue trace in the bottom panel). During this time period, we ramp the gate voltage of  $SEB_0$  (top panel) to change the charge state of the SEB, while the gate voltage on  $SEB_1$  remains static (middle panel). For  $400 \text{ ms} < t < 660$  ms, we deselect the MUX. For  $t > 660$  ms, we select MUX:1 and detect charge oscillations in  $SEB_1$  swapping the voltage profiles on the SEB gates. We record the data while the corresponding gate voltage is being ramped up (time windows between the

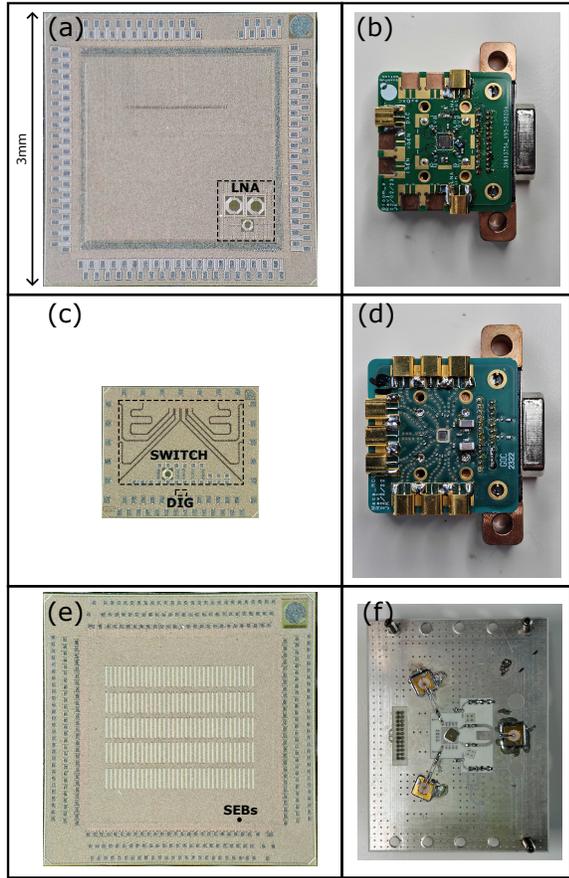


Fig. 3. Chips and Modules. (a) LNA IC micrograph. (b) LNA module photo. (c) Switch IC micrograph. (d) Switch module photo. (e) Quantum dot array IC micrograph. (f) Quantum dot array module photo.

vertical dashed lines).

Next, we benchmark the sensitivity of the assembly in terms of the power signal-to-noise ratio (SNR). We define the signal as the square of the voltage amplitude of a SEB oscillation as measured in the IQ plane and the noise as the square of the average standard deviation of the voltage levels at the top and bottom of the oscillation. We find a  $\text{SNR} = 140$  at  $10 \mu\text{s}$  integration time, corresponding to an integration time for  $\text{SNR} = 1$  of  $70 \text{ ns}$ . The result indicates that, with our methodology, high-fidelity readout of silicon spin qubits could be achieved in timescales well below  $10 \mu\text{s}$ , a results that compares favourably to previous demonstrations [2], [6] and fulfills the readout requirements to implement a fault-tolerant quantum computer.

## CONCLUSIONS

We have demonstrated a multi-module assembly for RF readout of silicon QD devices where all chiplets have been manufactured using the GlobalFoundries 22FDX process. In the demonstration, we include a RF switch for the delivery of time-division multiplexed high-frequency signals to an array of single-electron box charge sensors, whose transmitted signal is 50-ohm matched and amplified using a cryogenic low-

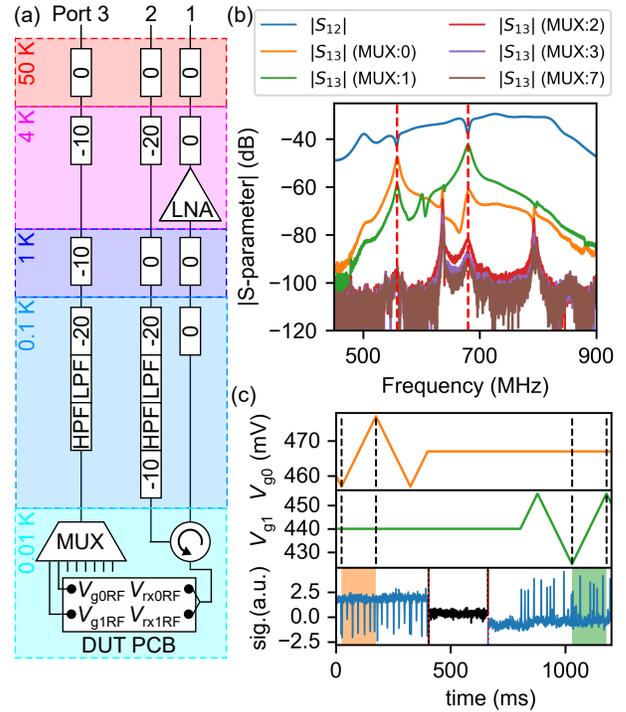


Fig. 4. Multi-chip assembly and cryogenic setup. (a) Cryogenic setup placed inside a dilution refrigerator. Rectangles indicate attenuation or low- or high-pass filtering stages. (b) S-parameter characterisation. The different traces correspond to the  $|S_{ij}|$  (MUX: $k$ ) where  $i(j)$  refers here to the output(input) port and  $k$  to the active MUX output channel. (c) Time-division multiplexing. Top panel and middle panels indicate the time-dependent voltage applied to gate 0 and 1 respectively. Bottom panel: Time trace of the demodulated signal.

noise amplifier. We benchmark the sensitivity of the assembly and find a power SNR of 140 for a readout time of  $10 \mu\text{s}$ , approaching state-of-the-art values [7]. Our results highlight the potential of CMOS technology towards the realisation of a quantum computing system containing not only quantum devices but also cryogenic analog and digital electronics.

## ACKNOWLEDGMENT

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